A 1024 K, 2/6 MHz H/Z-89 COMPUTER

by Leon A. Wittwer

I. Introduction

This article introduces the modifications for converting a H/Z89A (H/Z89) with 64 kilobytes of memory and a 2 megahertz CPU to 1024 kilobytes of memory and a 2/6 megahertz CPU. The extra memory and speed results in a computer that has all the properties of the H/Z89A's(H/Z89's) that have made it so popular, software, etc., along with the capabilities to be competitive with later generation home computers. I must point out, however, that my basic reason for these modifications is the same reason that people climb a mountain--because it is there. From prior hardware modifications of the H/Z89 for more memory (176 kilobytes) and faster speed(4 megahertz), it became clear that the potential of the H/Z89A (H/Z89) had not yet been fully realized. Of course, the availability of 256 kilobyte dynamic RAM's and a 6 megahertz Z80B CPU was the key to this project. All that remained was to develop a workable design within the constraints posed by the existing H/Z89A (H/Z89) hardware and software. This design is as conservative as I could make it. There are steps that are not strictly necessary, but were done to add design margin. The steps described here should take about 30 hours to execute. The total cost is less than $140 with the memory chips costing about $100 and the rest being for sockets, wire, etc. Extra CPU boards are available for an extra $100.

The 2/6 megahertz modifications result in some minor changes in the CPU board operation. Occasionally when turning on, two "H:" prompts will appear. This is no problem. Proceed as usual. The memory available can not be jumpered back to less than 64 kilobytes of RAM. An option has been included to remove the single step procedure if not used. Does anyone ever use this feature? Finally the read only feature for the static RAM has been disabled. These changes should have no effect on normal HDOS or CP/M operation.

The author makes no guarantee that the modifications stated here will work on another machine. As such, the author is not financially liable or liable in any other way for the failure of these modifications. It is strongly recommended that the reader work on spare boards for these upgrades. The author will provide reasonable advice and consultation (as determined by the author) to assist in implementation. The author has successfully implemented these steps with five CPU boards (and they all work).

The complete set of instructions has been submitted to the Capitol Heath Users' Group software library in HDOS and CP/M versions. The files provided under HDOS include: the hardware modification instructions, H17 and H47 6 Mhz drivers, a RAM disk driver and initializer, a direct extra memory access routine for HDOS, Microsoft Fortran, and a memory test routine that tests all 1024K of dynamic RAM. The files provided under CP/M includes: the hardware modification instructions, a BIOS.ASM(CP/M 2.203) file with simulated RAM disks, a direct extra memory access routine for CP/M Microsoft Fortran, and a memory test routine that tests all 1024K of dynamic RAM. The BIOS.ASM has the new portions clearly marked so that the changes can easily incorporated into other BIOS source files with a bit of editing.

The author on request will provide a set of drawings that show the key functions for this design. These are useful if the user wishes to understand why various steps are done. The author is much faster in answering requests for these drawings, software, or other information about the modifications if blank disks, self-addressed stamped envelopes, etc. are provided. Phone calls are accepted at (703) 960-2337 during civilized hours: 0800 to 2100 eastern time. Remember, this is a non-profit hobby operation so cooperation is a strong function of the personality of the requestor. My address is: Dr. Leon A. Wittwer, 5713 Lawsons Hill Court, Alexandria, Va 22310

II. Hardware Modifications

The hardware modifications provide for two separate upgraded capabilities. The first is the 1024K memory capacity and the second is the 2/6 megahertz CPU clock. The instructions permit either or both to be implemented. These modifications involve the CPU board and the 16K Memory Expansion Accessory. It is recommended that the Heath expansion board be used as it has adequate space for most of the extra circuitry necessary. The modifications involve removing traces, adding extra wiring, removing unnecessary parts, and adding sockets with associated wiring. These changes require reasonable skill with a soldering iron, considerable patience, and a knack for reading and following directions.

The CPU clock is controled via port 362Q. The following bytes provide for 2/6 megahertz.

Clock Rate(MHZ)	Port 362Q Data
2	XXX0XXXX
6	XXX1XXXX

On RESET, the computer comes up at 2 megahertz. This provides for booting with standard ROM's. After booting, the clock can be software switched to the desired rate assuming that the system software can handle the speed. The standard Heath ROM's and static RAM can be read and written to at both speeds since wait states are inserted when accessing the lower 8 kilobytes of memory under HDOS. Wait states are also provided for all input/output operations. The clock lines on P510, P511, and P512 remain at 2 megahertz. Some modest changes may be necessary on boards that are used at P510 through P512.

The new memory is accessed by controling bit 5 of port 362Q and all bits at port 077Q. Setting bit 5 of port 362Q enables dynamic RAM access for the lower 8 kilobytes of the Z80 address space. Otherwise the lower 8 kilobytes access the static RAM, the Monitor EPROM, and the H17 PROM. For the remainder of this discussion, bit 5 of port 362Q is assumed set to one.

The address byte for port 077Q is of the form: IIIIJJJJB. IIII has the four extra address bits for the 256 kilobit dynamic RAM chips on the CPU board. JJJJ performs the same function for the memory on the 16K Memory Expansion Accessory. This scheme allows 15 banks of 64K memory in addition to the normal Z80B address space.

At reset, the new address bits are reset to zero. Thus 00000000B is the address of the operating system and user programs. Under HDOS, bit 5 of port 362Q is normally not set. The software sets this bit at the correct time to access all the extra RAM. Under CP/M, the bit is set permanently.

III. Software

The use of 6 megahertz requires changes to the H17 and H47 drivers under HDOS. Modified drivers are have been developed . The H17 driver supports 400K hard sector outboard drives in addition to the standard 100K drives. When booting with either the H17 or the H47, the clock is switched to 6 megahertz when the SY0: driver is loaded. Switching to a slower speed is only required for some games and other time dependent software. Remember that the H17 and H47 will only be reliable at the speed associated with the driver being used. The RAM disks (to be discussed) come in handy here as they are useable at any CPU speed. For CP/M, the latest BIOS80 (Version 5) from Livingston Logic Labs supports 6 megahertz operation for both the H17 and the H47. For both HDOS and CP/M, the simplest procedure is to switch to 6 megahertz on boot. For CP/M, the switching can be done by inserting the following instructions:

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ORI 16
MOV M,A
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after

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LXI H,CTLPRT
MOV A,M
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which are located a few instructions after the CBOOT: label in the BIOS.ASM file. It is useful to build BIOS.SYS files for each clock speed where the 6 megahertz version is described above and the 2 megahertz version has an "ORI 0" instruction replacing the "ORI 16" instruction. You can then pick the speed after booting by using the correct BIOS.SYS. (You need the "ORI 0" and the "MOV M,A" instructions so the different BIOS.SYS files are the same size.)

The author does not support the H37. There are CPU clock dependences in routines H37ISR, RESH371, RDYH37, and WBS37 in the CP/M 2.2.04 BIOS. There are likely such dependences in the HDOS driver. Also, since the P510, P511, and P512 busses are at 2 megahertz independent of the CPU speed and that the H37 interface board plays games with the interrupts, there may be hardware issues regarding the H37 interface board. The author would be willing to attempt to resolve these issues if anyone provides the necessary H37 data.

The extra memory is accessed in two modes. First, the memory can be accessed as fast disks. The EC.DVD driver and the INITEC program has been written to provide this capability under HDOS. INITEC initializes up to three fast disks from the available RAM. A modified BIOS is available for CP/M which also lets the user configur up to three RAM disks from the available RAM. This software is transparent to interrupts 1(clock), 3(console), 4, and 5 in HDOS and interrupts 1(clock), 3(console), and 4 in CP/M. Additional interrupts can be accommodated if required. This software moves a byte from the disk/memory to the memory/disk in less than 23 clock cycles. The minimum addressable unit of memory is 256 bytes under HDOS and 128 bytes under CP/M.

The second mode of memory access is called Extended Core Storage. This is direct access from within Microsoft Fortran programs using a Fortran routine. The memory appears as blocks of 32768 4 byte words. The minimum addressable unit of memory is 4 bytes although this is somewhat slow. If a number of words are accessed, the data can be moved at rates similar to that for the fast disk.

The extra memory can be allocated between the fast disks and the ECS. This provides storage for data without the extra disk overhead and disk storage for overlaying program code. In general any memory not allocated to the RAM disks will be available to the ECS.

IV. Final Comments

I hope that those who implement a 6 megahertz, 1024K computer will have as much enjoyment as I did. Sometimes, I think that most of of the fun was in working the changes and not the result. It is, however, rather nice to run most software at least three times faster and to have large amounts of very fast memory available. I encourage others to figure out how I did the redesign and look forward to suggestions as how to do things differently or better. Ideas for software that utilize the extra memory are also sought.

THE DIRTY DOZEN ISSUE #6

This is a Program Alert List Downloaded from DIANA, the Naval Aviation Bulletin Board. it was originially compiled by Tom Neff with Updates by Eric Newhouse & Gerhard Barth. Recently, many unlawfully copied or modified programs have appeared on various IBM PC bulletin boards across the country. THE DIRTY DOZEN is a list of known examples. If you have any additions or corrections for this list, please contact Gerhard Barth.

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ZDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD?
3 Special Warning!                                        3
3    Added to Trojan List on 6-29-86:  QUICKREF.ARC       3
3    which contains the Trojan horse ARC513.COM. Careful! 3
3                                                         3
3    ARC512 online (on DIANA) is the current version and ok.3
@DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDY
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NOTE: If no file extension is supplied, that means that the file has been circulating under many different extensions. For instance, BALKTALK has been seen with extensions of: .EXE, .COM, .EQE, .CQM, .LBR, .LQR, and .ARC.

HACKED & TROJAN HORSE PROGRAMS:

Name	Category	Notes
ARC.COM		This is an unauthorized modification
ARC513.EXE	*TROJAN*	This hacked version of arc appears normal, so beware! It will write over track 0 of your [hard] disk upon usage, destroying the disk.
BALKTALK	*TROJAN*	This program used to be a good PD utility, but some one changed it to be trojan. Now this program will write/destroy sectors on your [hard] disk drive. Use this with caution if you aquire it, because it's more than likely that you got a bad copy
DISKSCAN.EXE	*TROJAN*	This was a PC-MAGAZINE program to scan a (hard) disk