THE SIGMASOFT DISK SYSTEM

USERS MANUAL

Second Edition

SigmaSoft and Systems

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The SigmaSoft Disk System is an integrated hard/floppy disk controller, H/Z89 or H8 interface, HDOS and CP/M support package. This package allows H/Z89 and H8 users to take full advantage of the very latest in mass storage technology.

The interface board connects to either the H/Z89 or H8 computer bus and provides 16 parallel I/O ports. Eight of these ports are for communication with the Western Digital 1002 controller board which is mounted to the side of the first hard disk drive in the system. The remaining eight ports make up the interface to the Interactive Graphics Controller and the two printer interfaces. Four jumpers are present on the interface board to allow the selection of any port address for the interface.

The WD1002 controller is both a hard disk controller and a floppy disk controller. The hard disk interface supports up to three ST506 compatible drives with each drive being limited to a maximum of 1024 cylinders and 8 recording heads. An on board microprocessor monitors and reports error conditions using an ECC (Error Correction Coding) polynomial. The floppy interface portion of this board supports up to four SA450 compatible drives with each drive being limited to a maximum of 80 tracks and 2 recording heads. Both single and double density recording are supported.

The supplied drive unit is either a 10 or 20 megabyte capacity Winchester hard disk with either 2 or 4 recording heads and at least 305 cylinders. 3.5 inch half height drives are used for systems to be mounted in the H/Z89's internal drive mounting slot, while 5.25 inch half height drives are used for externally mounted systems. A small white label is present on all drive systems indicating the manufacturer and model number of the actual drive unit.

The software supplied with each system consists of SigmaBIOS, a BIOS replacement for the standard Heath CP/M, hard and floppy drive device drivers for both HDOS and CP/M, and numerous other utilities for installing and maintaining the disk system under these two operating systems. The SigmaROM MTR-90 replacement boot ROM is also provided for H/Z89 systems to allow cold booting of the WD1002 controller without the use of other disk systems.

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Manual Scope

This manual has been provided to aid the user in installing preparing, organizing, using, and servicing the SigamSoft Hard/Floppy Disk System. It describes these operations with reasonable clarity and detail for the owners of an H/Z89, H/Z90, H8, or H-1000 type microcomputer equipment running either the Heath HDOS or CP/M operating systems.

By no means is this manual intended to be a tutorial of either the HDOS or CP/M operating systems. Both of these systems are far to complex to fully describe in this manual. The author assumes that the user is familiar with the operating system that he or she is running. If not, it is strongly recommended that you consult the original Heath documentation on their software products.

The following section details the first steps of installing an internal mount disk system. If you purchased a disk system which is mounted in its own external cabinet, then skip this section and proceed to the installation of the Interface Board.

The internal mount disk system is intended for use in the front of an H/Z89 cabinet, although it can also be mounted into the front of an H/Z19 terminal if you have also installed the proper H/Z89 type power supply and drive mounting bracket. The parts to do this are available from the Heath Company.

Step #1, Getting Started

To begin the installation of the internal mount disk system, position the H/Z89 or H/Z19 on a table with the cover removed. It may require a screwdriver to release the two side latches which fasten the cover closed. Turn the H/Z89 or H/Z19 so that the right side (from the front) is positioned comfortably in front of you.

Refer to Illustration A during the process of installing the Power Supply Board. Please be sure to read each step completely before performing any part of that step.

Step #2, Disk Drive and Shield Removal

If a disk drive unit is already present in the front of the H/Z89 cabinet, it must now be removed to make room for the hard disk unit. This will also provide access to the mounting holes for the Power Supply Board installation. The drive is released by removing two screws from the top, two more screws near the bottom, and two cables that connect to the drive unit's circuit board in back. The drive unit can then be pulled out from the front of the H/Z89 cabinet. If you wish to continue using the drive unit you have just removed, it can now be mounted in an external drive cabinet.

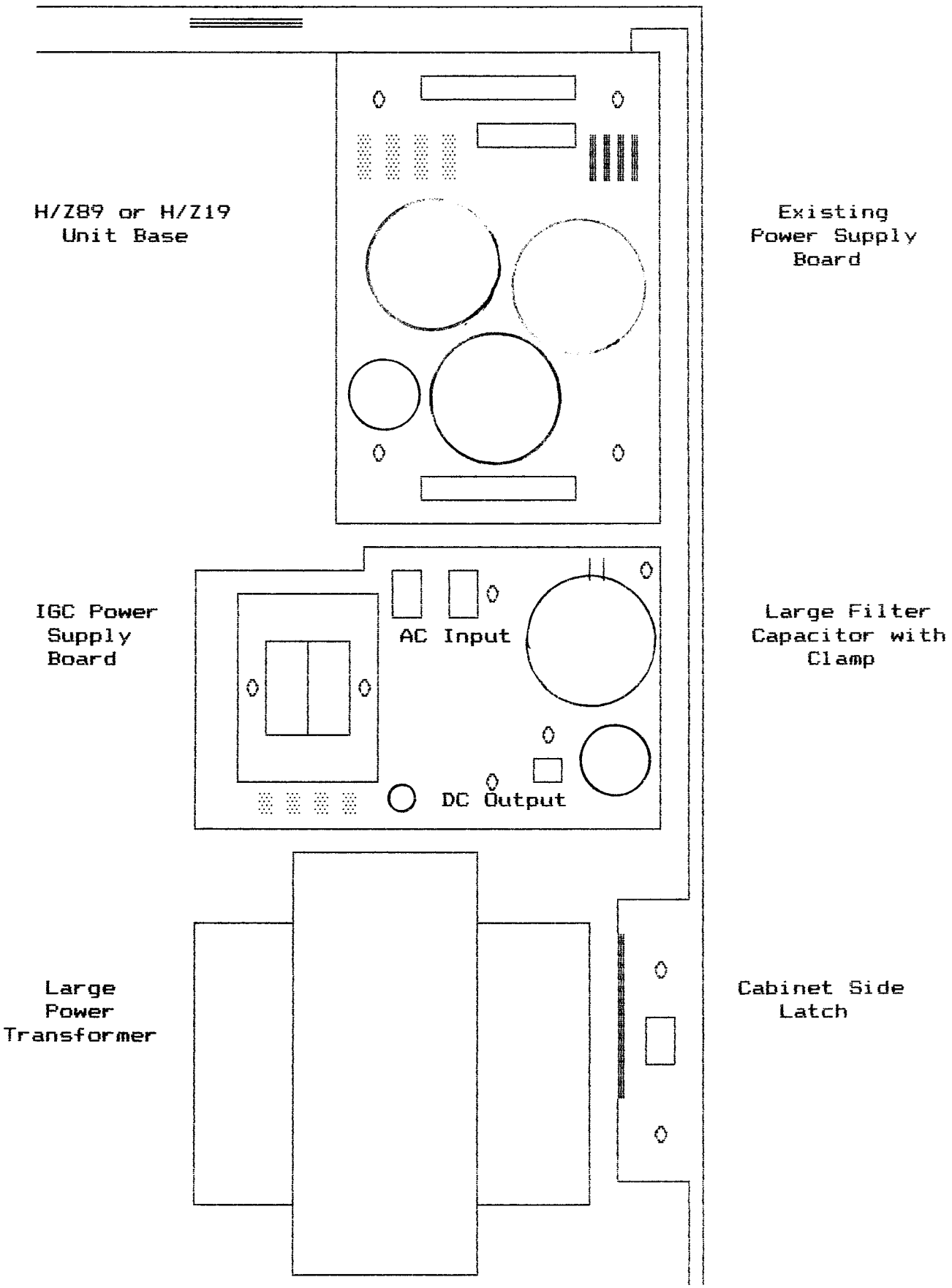
Next, remove the drive unit shield. This shield either partially or completely surrounded the drive unit before it was removed. The shield may be held in place by 4 screws that fasten it to the front of the H/Z89 unit. Set the shield aside until needed. Note that in some cases the disk drive shield and the drive mounting bracket are the same component.

Step #3, Filter Capacitor Removal

Locate the large filter capacitor which is mounted in the base of the H/Z89 or H/Z19 directly beside the power transformer. The top of this capacitor may be covered by a blue plastic insulator. The filter capacitor is mounted to the base with a capacitor clamp and has four connecting wires, colored blue and black.

Use a screwdriver to remove the two screws which fasten the capacitor clamp to the base, but do not remove the clamp or the wires from the capacitor.

Illustration A



Lift the capacitor (with clamp and wires attached) out over the side of the H/Z89 or H/Z19 base. Carefully, pull the filter capacitor out as far as possible to provide sufficient wire length to work with.

In some cases there may be an uninsulated ground strap connecting to the capacitor clamp and screwed to the base of the H/Z89 or H/Z19 cabinet. If it is present, disconnect it from the filter capacitor clamp.

Step #4, Filter Capacitor Remounting

Attach the filter capacitor to the new Power Supply Board with two #6 screws, two #6 lock washers, and two #6 nuts. Be sure that the filter capacitor is attached to the component (not foil) side of the new Power Supply Board and that the blue and black wires attached to the capacitor are routed away in the direction of the top of the board.

Step #5, Power Supply Board Mounting

During the following step, check to be sure that no metallic objects are close enough that they might make contact with the foil side of the new Power Supply Board once it has been installed. There may be grounding straps and solder lugs attached to the filter capacitor clamp and/or the power transformer. These must either be removed or positioned away from the new Power Supply Board or they will create a severe short circuit hazard.

If a bare ground strap cable is present, it must be insulated. Fasten it to the base of the H/Z89 or H/Z19 unit with the adhesive insulating tape that was provided. Position the cable so that it does not pass underneath the new Power Supply Board.

Slowly position the new Power Supply Board into the base of the H/Z89 or H/Z19 at the same position at which the filter capacitor was mounted. This step requires some care and patience, as the board must be worked through the many wires and cables in the way. The new Power Supply Board should be positioned so that its two mounting holes are directly above the mounting holes in the base at which the filter capacitor was attached, with the small transformer on the board toward the interior of the H/Z89 or H/Z19 unit.

Do not be afraid to pull the bulk of wires in this area up out of the way so that this board can be mounted. Feel free to cut any wire ties (DO NOT CUT ANY WIRES) needed to ease this operation. Replacement wire ties are provied for rebundling the wires after installation.

Once installed, there should be no wires beneath the new Power Supply Board. These wires should be routed over the top of the two large filter capacitors on this board.

Use two #6 screws and two #6 lock washers to fasten the new Power Supply Board to the H/Z89 or H/Z19 base using the same two mounting holes that the large filter capacitor clamp was originally mounted to. Note that a 3/8 inch #6 screw must be used at the mounting hole near the AC power connectors while a long 1 and 1/4 inch screw must be used at the other mounting hole to reach through the voltage regulator heat sink.

Step #6, Power Supply Cables Installation for the H/Z89

If you are installing the new Power Supply Board into an H/Z19 and not an H/Z89, skip this step and proceed to Step #7.

Locate the 3 power supply cables that were provided. One of these cables has a 2 pin connector at one end and a four pin connector shell at the other, this is the Disk Controller Power Cable. The other two cables have 3 pin connectors, they are the AC Line Input Cables. Note that some of the pin positions of the connector shells on these cables are unused, but are considered to be present when determining the pin count of a connector shell.

Begin by connecting the 2 pin end of the Disk Controller Power Cable to the 2 pin output connector on the new Power Supply Board. The other end of this cable will be connected to the Disk Controller, later.

WARNING! Take extreme care when connecting cables to the new Power Supply Board. Never join two connectors of an unequal number of pins. Never join two connectors unless they fit together easily without force. The single 2 pin connector on this board is the low voltage output, it must never be confused with the two 3 pin AC line connectors (high voltage).

Each of the 3 connectors on the new Power Supply Board has a locking ramp for polarization. Each time a cable is connected to one of these connectors be absolutely certain that the ramp on the connector of the cable is positioned toward the ramp on the connector of the circuit board that it joins with. The slots in the connector on the cable's end must always be positioned away from the ramp on the circuit board's connector.

Next, locate the AC line cable that connected to the fan before the H/Z89 cover was removed. This cable comes through an opening in the unit's base under the existing power supply board. Join the free end of this cable with the short (about 3 inches) AC Line Cable. Only the end of this cable without the locking ramp can be connected to the fan cable.

Now, connect the other end of the short AC Line Cable (the end with the locking ramp) to one of the two 3 pin AC Line Input connectors on the new Power Supply Board. These two 3 pin AC Line Input Connectors are interchangeable.

Connect the long AC Line Input Cable to the other 3 pin AC Line Input Connector on the new Power Supply Board, just as the short cable is connected. The free end of this long cable will now be your fan cable.

Step #7, Power Supply Cables Installation for the H/Z19

If you are installing the new Power Supply Board into an H/Z89 and not an H/Z19, skip this step and proceed to step #8.

Locate the 2 power supply cables that were provided. One of these cables has a 2 pin connector at one end and a four pin connector shell at the other, this is the Disk Controller Power Cable. The other cable has a single 3 pin connector at one end, this is the AC Line Cable. Note that some of the pin positions of the connector shells on these cables are unused, but are considered to be present when determining the pin count of a connector shell.

Begin by connecting the 2 pin end of the Disk Controller Power Cable to the 2 pin output connector on the new Power Supply Board. The other end of this cable will be connected to the Disk Controller, later.

WARNING! Take extreme care when connecting cables to the new Power Supply Board. Never join two connectors of an unequal number of pins. Never join two connectors unless they fit together easily without force. The single 2 pin connector on this board is the low voltage output, it must never be confused with the two 3 pin AC line connectors (high voltage).

Each of the 3 connectors on the new Power Supply Board has a locking ramp for polarization. Each time a cable is connected to one of these connectors be absolutely certain that the ramp on the connector of the cable is positioned toward the ramp on the connector of the circuit board that it joins with. The slots in the connector on the cable's end must always be positioned away from the ramp on the circuit board's connector.

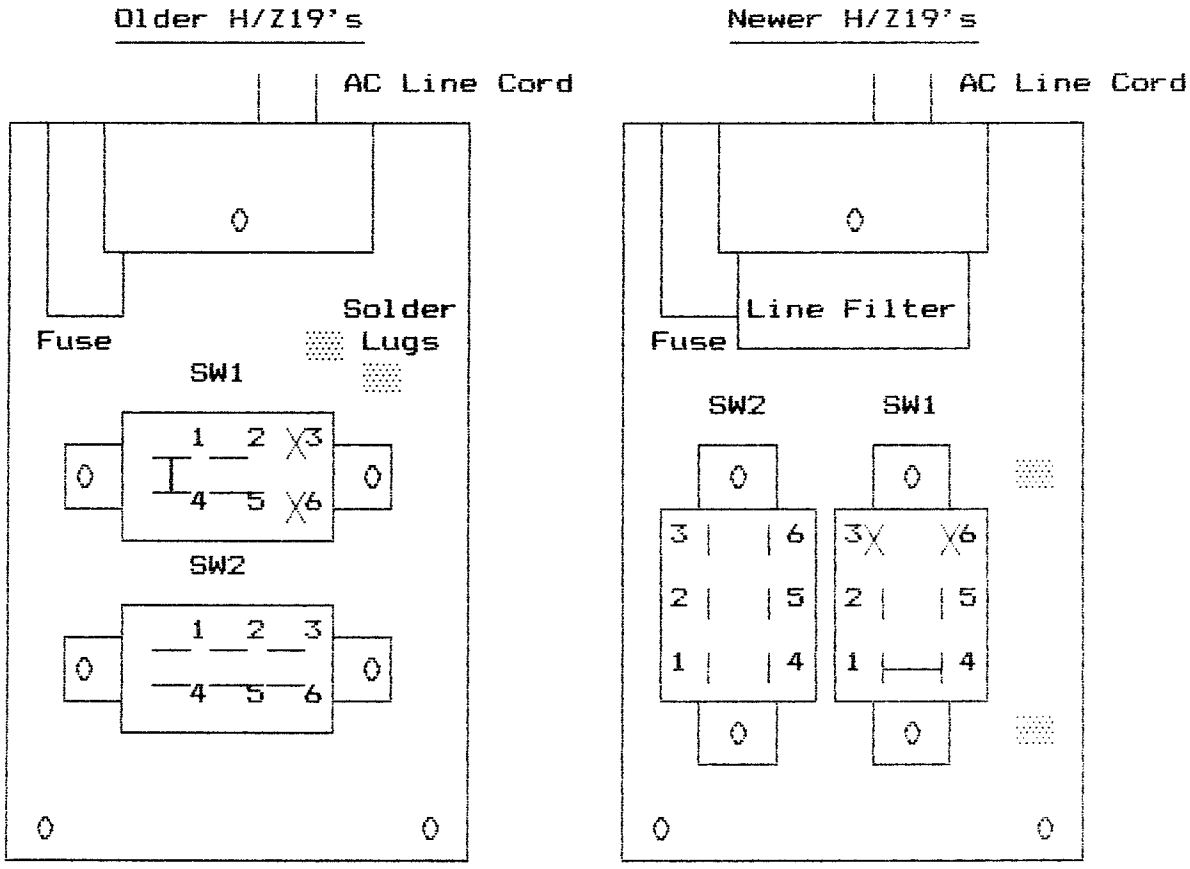
Remove the two screws that hold the chassis cover in place over the AC section of the H/Z19 power supply. This is the metal piece in which the unit's power switch and fuse are mounted. Gently pull the chassis cover outward to provide access to the solder lugs of the 115V/230V Switch (SW1). This switch is mounted on the bottom of the H/Z19 unit. Do not confuse it with the main power switch (SW3) or the low voltage switch (SW2).

Connect the AC Line Input Cable to either of the 3 pin connectors on the new Power Supply Board. Route the bare end of this cable through the opening in the H/Z19 base into the AC power section. This opening is located underneath the H/Z19 power supply.

Note that in the following step the AC Line Input Cable will be soldered onto 2 of the solder lugs on switch SW1. In some cases this switch may be positioned horizontally above SW2, or it may be mounted vertically beside SW2. Refer to Illustration B to identify SW1 and the 2 solder lugs at which the AC Line Input Cable is to be attached. The correct solder lugs have been indicated with two X symbols in the illustration.

Solder either of the two bare ends of the AC Line Input cable onto lug number 3 on SW1. Solder the other bare conductor of this same cable onto lug number 6 of SW1. Carefully inspect the solder connections you have just made to be sure that they are correct, and that all of the solder lugs are well insulated from one another. Then, reinstall the chassis cover of the AC section of the H/Z19 power supply.

Illustration B



Step #8, Power Supply Installation Tests

Reinstall the H/Z89 or H/Z19 cover so that the new Power Supply Board can be tested. Join the long AC Line Input Cable with the fan cable in the unit's cover, if present. Once again, inspect the AC lines and be sure their connection to the new Power Supply Board is correct. Then, close the cover of the H/Z89 or H/Z19 and plug the AC line cord into a wall socket.

Turn on the power switch to the H/Z89 or H/Z19. The unit should begin operating as usual. If not, turn the power switch off and check the unit's fuse. A blown fuse is an indication of an installation error.

If you have a voltmeter, test the output of the new Power Supply Board at the free end of the Disk Controller Power Cable. This is the 4 pin connector shell with two conductors. The measured voltage must be between 4.75 and 5.25 Volts DC. Do not proceed any further with the installation of the hard disk system unless the new Power Supply Board operates properly.

Step #1, Interface Board Installation for an H8

If you are installing the Universal Parallel Interface Board into an H/Z89 and not an H8 computer, skip this step and proceed to Step #2.

The installation of the H8 version of the Interface Board is very straightforward. Simply connect the board to any available bus slot inside the H8 mainframe. Refer to the Configuration section for information on setting the various jumpers on this board. If you have any special accessory cables to install, such as a Centronics printer cable, proceed to the accessories installation section. Otherwise, proceed directly to the Hard Disk Drive installation section.

Step #2, CPU Logic Board Removal

Start by removing the CPU Logic Board from the H/Z89 unit. The CPU Logic Board is the large board mounted vertically directly behind the CRT of the H/Z89. The smaller boards which are attached to the CPU Logic Board may remain attached.

Several cables must be detached from the CPU Logic Board and the smaller boards to facilitate their removal. Be sure to take note of how these cables are connected so that you can reconnect them properly once this installation proceedure is complete.

Step #3, Mounting Hardware Removal

In some cases there may be a Support Bracket that connects the CPU Logic Board to the front of the H/Z89 cabinet, just above the CRT. Remove this bracket if it is present.

Locate the Accessory Mounting Brackets that connect to the top of the CPU Logic Board to support the smaller accessory boards. There may be just one located on the right side, or a second one on the left side. If an Accessory Mounting Bracket is present on the left side, remove it. This bracket will no longer be needed. Do not remove the mounting bracket on the right side.

Step #4, Interface Board Installation

Plug the Universal Parallel Interface Board onto one of the 3 bus slots on the left side of the H/Z89 CPU Logic Board. Any of the 3 left side slots can be used. They are numbered P501-P507, P502-P508, and P503-P509. This board cannot be connected to any of the 3 bus slots on the right side of the CPU Logic Board.

Note that an H-1000 CPU board has a single left bus slot which is a double row of pins. If you are installing the interface board onto an H-1000 type CPU board, plug the board in so that it only uses the left most row of pins on the bus connector.

Step #5, CPU Control Cable Installation for an H/Z89

If you are installing the Universal Parallel Interface Board into an H-1000 system, skip this step and proceed to step #6.

Locate and remove the Integrated Circuit U553 from its socket on the CPU Logic Board. It's the first IC to the left of the DIP switch (SW501), near the bottom right corner of the CPU Logic Board. Check to be sure that the IC chip you have removed has 14 pins and bears the part number 74LS32. The part number may not match exactly, but it should be close.

Locate the CPU Control Cable. This cable has a single 8 pin connector at one end and a black 14 pin DIP plug at the other. Note that one corner of the DIP plug is notched to indicate pin 1.

Plug the black DIP plug of the CPU Control Cable into the U553 socket. Be sure to position pin 1 of the DIP plug so that it connects to pin 1 of the U553 socket. Pin 1 should be labeled on the CPU Logic Board beside the U553 socket. Once connected, the small wire attached to the DIP Plug should exit from the top. The IC chip removed from U553 will no longer be needed.

Connect the free end of the CPU Control Cable to the 8 pin connector at the top right corner of the Interface Board. This connector must be positioned so that the 3 conductor cable enters the 8 pin connector shell on the right side. The 8 slots cut in the body of the connector shell must be positioned up and not down. Also note that this cable should be routed over any other circuit boards which obstruct its path, and not under them. This is because of the high voltages radiated by the Flyback Transformer which is located underneath the Interface Board.

Step #6, CPU Control Cable Installation for an H-1000

If you are installing the interface board onto an H/Z89 CPU Logic Board, and not an H-1000 CPU board, skip the following step and proceed to Step #7.

Due to differences in the design of the H-1000 CPU board, the three conductors of the CPU interface cable must be soldered directly to the solder side of the CPU board. Refer to the chart below to connect these three wires.

Required Signals for Operation with an H-1000 CPU Board

Board Connector	Signal Name	CPU Board Part	Pin Number
1	Inverted M1	U591	3
2	I/O Enable	U509	9
3	Read Enable	U509	5
4			
5			
6			
7			
8			

Connect the free end of the CPU Control Cable to the 8 pin connector at the top right corner of the Interface Board. This connector must be positioned so that the 3 conductor cable enters the 8 pin connector shell on the right side. The 8 slots cut in the body of the connector shell must be positioned up and not down.

Step #7, CRT Anode Socket Positioning

Locate the CRT anode socket and high voltage cable that connects the anode socket to the flyback transformer. The CRT is the picture tube of the H/Z89 computer and the flyback transformer is the black circular object located directly below the interface board. The cable that connects between them must be positioned as far away from the interface board as possible. To accomplish this, the anode socket connector on the CRT should be rotated to point downward. The anode socket will turn if the plastic insulator covering it is gently squezed.

Step #8, Interface Board Testing

This completes the installation of the Universal Parallel Interface Board. If you purchased a Centronics printer cable to use with the interface board, proceed to the accessories installation section first and install these cables before you reinstall the CPU Logic Board. Otherwise, you should now reinstall the CPU Logic Board to test the operation of the computer with the interface board in place.

The CPU Logic Board will be removed again to install the SigmaROM. However, it is very important that the operation of the computer be tested with the interface board in place before the ROM is installed.

Carefully check to be sure that all of the cables to the CPU Logic Board are reconnected as they were before. Apply power to the H/Z89 and test it for normal operation. If the computer does not operate as normal, then turn the power switch off and thoroughly recheck your installation. If the operation is normal, then proceed to install the SigmaROM.

The following section details the installation of the SigmaROM (MTR-9Ø replacement) for the H/Z89. This ROM allows the user to boot HDOS and CP/M from the SigmaSoft Hard/Floppy Disk System without the use of existing floppy drives. However, this ROM is not required to use the SigmaSoft disk system and its installation is optional. Furthermore, if your H/Z89 does not currently have an MTR-9Ø ROM (but the older MTR-88 or MTR-89 ROM instead), then your computer will not operate with the SigmaROM without making the proper Heath modifications to bring it up to date. To determine which type of ROM you have, read Step #2 carefully.

The only disadvantage to installing the SigmaROM is that your H/Z89 will no longer be able to boot a Heath Z67 drive system.

Step #1, CPU Logic Board Removal

Start by removing the CPU Logic Board from the H/Z89 unit. The CPU Logic Board is the large board mounted vertically directly behind the CRT of the H/Z89. The smaller boards which are attached to the CPU Logic Board may remain attached.

Several cables must be detached from the CPU Logic Board and the smaller boards to facilitate their removal. Be sure to take note of how these cables are connected so that you can reconnect them properly once this installation proceedure is complete.

Step #2, Monitor ROM Removal

Locate and remove the Monitor ROM on the CPU Logic Board. This ROM (often referred to as MTR-9Ø) is labeled on the circuit board as U518. It is a 24 pin EPROM with a small quartz window which may be covered by a paper label. If this paper label is present, it should bare the Heath part number of either 444-84 or 444-142.

On some older models of the H/Z89, this part number may be different (an MTR-88 or MTR-89 is present). If this is the case with your H/Z89 then the ROM should not be removed and the SigmaROM can not be installed without first changing the secondary address decoder which is located at U516 and making some jumper changes on the CPU board as well. The chart below summarizes.

ROM Compatibility Summary

ROM Name	Heath Part at U518	Required at U516	SigmaROM Compatible
MTR-88	444-4Ø	444-41	No
MTR-89	444-62	444-41	No
MTR-9Ø	444-84	444-83	Yes
MTR-9Ø	444-142	444-83	Yes

There are four jumper wires on the H/Z89 CPU Logic Board which are associated with the above components. These are either labeled as JJ5Ø5, JJ5Ø6, JJ5Ø7 and JJ5Ø8, or JJ5Ø4, JJ5Ø5, JJ5Ø6, and JJ5Ø7. These should be set as follows:

Summary of CPU Board Jumper Settings

Older H/Z89's Newer H/Z89's	JJ5Ø5 JJ5Ø4	JJ5Ø6 JJ5Ø5	JJ5Ø7 JJ5Ø6	JJ5Ø8 JJ5Ø7
MTR-88 or MTR-89	Ø	Ø	Ø	1 (or B)
MTR-9Ø or SigmaROM	1	Remove	1	1 (or B)

Note that a jumper wire must also be installed between the center pin of JJ5Ø5 (or JJ5Ø6 on older H/Z89's) and pin 14 of P5Ø8 to use either MTR-9Ø or the SigmaROM. This jumper should already be present if you have an MTR-9Ø ROM. The required secondary address decoder mentioned above can only be obtained from the Heath Company (part number #444-83).

Care should be taken when handling these ROM devices as they are static sensitive and can be damaged easily. These devices can be protected by placing them into black conductive foam or aluminum foil.

Step #3, SigmaROM Installation

Remove the SigmaROM from the protective foam and note the small indentation on one end of the component. Check the pins of the ROM to be sure that they are straight, and plug the ROM into the 24 pin socket at U518 with the small indentation positioned at the same end as the white dot on the circuit board under the socket.

The installation of the SigmaROM alters the definition of some of the DIP switch settings at SW5Ø1 on the CPU Logic Board (especially if you have been using the older MTR-88 or MTR-89 ROMs). Refer to the Configuration section of this manual to reprogram these switches for proper operation.

Step #4, CPU Board Reinstallation

Plug the MTR-9Ø ROM you removed earlier into the static protective foam and save this part for possible future use. This completes the installation of the SigmaROM you should now reinstall the CPU Logic Board to test the operation of the computer with the new ROM in place.

Carefully check to be sure that all of the cables to the CPU Logic Board are reconnected as they were before. Apply power to the H/Z89 and test it for normal operation. If the computer does not operate as normal, then turn the power switch off and thoroughly recheck your installation. If the operation is normal, then proceed to install the hard disk drive unit.

Step #1, H/Z89 Hard Disk Backplate Cable Installation

The following steps detail the installation of a hard disk drive unit which has been provided in a cabinet that is external to the H/Z89. If you purchased an internal mount system, proceed to Step #3. If you purchased an H8 system, proceed to Step #2

WARNING! During this installation proceedure, you will be handling the hard disk drive unit which is extremely sensitive to shock and vibration. These drives are typically rated by their manufacturer to withstand only 60 G's of shock without permanent damage. This amount of shock can be generated by dropping such a drive unit only a few inches onto a hard surface. Such a drop may trigger shock sensors inside of the drive unit which will void its warranty.

Locate the Hard Disk Interface Backplate Cable. This is a 34 conductor ribbon cable that simply extends the Hard Disk Interface Connector on the Interface Board to the backplate for easy access. Note that the installation of this cable requires a standard 34 pin drive cable mounting hole in the H/Z89's backplate which may not be available if you have an older model, or if you have already installed another drive cable that uses this mounting hole.

If a mounting hole is not available for this cable, you can either connect the interface cable from the external drive cabinet directly to the interface board, or use the backplate cable as an extension without mounting it to the backplate. In either case, the cable can be routed through any available opening in the back of the H/Z89.

If a mounting hole is available, position the H/Z89 on your workbench so that you are facing the back of the computer with the backplate hanging over the edge of the bench slightly. Use a screwdriver to remove the seven screws that mount the backplate to the H/Z89 base and gently pull the backplate outwards to provide access to the inside.

Use the provided hardware (#4 machine screws and nuts) to mount the male end of the backplate cable to the inside of the H/Z89 backplate so that the polarity notch is in the upward position. The cable should be routed underneath the CPU and Terminal Logic circuit boards to then be connected to the Hard Disk Interface Connector on the Universal Parallel Interface Board. This is the upper 34 pin connector on the edge of the board fartest from the CPU board. Note that this cable is polarized by a small notch to prevent improper installation.

Reinstall the H/Z89's backplate as it was before. The External Hard Disk Drive can now be connected to the H89's backplate with the 5 foot interface cable. Note that the 34 pin male connector mounted on the back of the external hard disk cabinet is the Z37 compatible floppy drive controller interface and should not be used at this time.

Step #2, External Hard Disk Installation

For either H/Z89 or H8 users, the external drive cabinet should now be connected to the interface board inside the computer. For H8 systems the 5 foot Hard Disk Interface Cable from the external drive cabinet must be routed through an opening in the rear of the H8 and connected to the Interface Board. The Hard Disk Interface connector on the Interface Board is the upper 34 pin connector for both the H/Z89 and H8 versions. The identical connector located below the Hard Disk Interface is the Interactive Graphics Controller Interface.

This completes the installation of the hard disk for external mount systems. Apply power to the drive unit and computer and test the computer for normal operation. Then proceed to the section on the Maintenance Software.

Step #3, Internal Hard Disk Installation

The following details the installation of a hard disk unit which has been provided without a cabinet to mount into the front of either the H/Z89 or H/Z19 cabinet. Note that the H/Z19 cabinet mounting requires that you have installed an H/Z89 type power supply and internal drive mounting bracket into the H/Z19 unit. The parts to do this are available from the Heath Company.

WARNING! During this installation proceedure, you will be handling the hard disk drive unit which is extremely sensitive to shock and vibration. These drives are typically rated by their manufacturer to withstand only 60 G's of shock without permanent damage. This amount of shock can be generated by dropping such a drive unit only a few inches onto a hard surface. Such a drop may trigger shock sensors inside of the drive unit which will void its warranty.

Begin by finding the three connectors on the hard disk controller board that will be used and note their location. This controller board is the larger of the two circuit boards that are attached directly to the hard disk drive unit. The large white nylon connector with 4 pins at the rear of the board is the Controller Power Connector (J6). There is an identical connector mounted on the drive unit beside the controller board. This is the Disk Drive Power Connector. It will also be used, so be careful not to confuse the two. The other important connector is located along the top edge of the board. The 40 pin connector (J5) is the Controller Interface Connector.

Note that the 34 pin connector (J8) is the Floppy Disk Interface Connector. If you have floppy disk drives you wish to interface through this controller, they must be connected here. Be sure to observe the pin 1 indications on the circuit board for both the 34 and 40 pin interface connectors.

Inspect the two cables that are already installed at J7 and either J1 or J3, to be sure that they are steated well at both ends.

Reinstall the disk drive mounting bracket into the front of the H/Z89 that was removed earlier to install the new power supply board. Slip the disk drive shield back into place around the drive mounting bracket. In some cases, the drive mounting bracket and the drive shield are the same component. If this is the case with your unit, this bracket must now be installed.

Locate the Controller Interface Cable and connect it to the Controller Interface Connector (J5) on the controller board. This cable has a 34 pin socket connector at one end and a 40 pin socket connector at the other. The end of this cable with the 40 pin connector should be connected so that the unused side of the socket connector is farthest from pin 1 of the 40 pin connector on the controller board. Note the small '1' or arrow on the circuit board that indicates pin 1.

A portion of this connector is unused in that only a 34 conductor ribbon cable is joined with the 40 pin socket connector. The unused or extra portion of this connector should be pointing toward the closest corner of the controller board.

Insert the loose end of the Controller Interface Cable in through the drive mounting hole in the front of the H/Z89 or H/Z19 cabinet. This cable will be connected to the Interface Board, later.

Gently slide the hard disk drive unit into the front of the H/Z89 or H/Z19 cabinet so that only the black plastic front bezel plate will be visible from the outside. The disk controller board should be on the left side (from the front of the H/Z89) and the large mounting bracket that surrounds the drive unit must be to the right. Perform this operation slowly to be sure that none of the components on the controller board are damaged.

Set the drive unit into the front mounting hole far enough that it won't fall back out, but not all the way in. Room will be needed behind the drive to connect the power cables.

Step #4, Power Cable Connections

Locate the free end of the Controller Board Power Cable that was installed onto the new Power Supply Board and connect it to the white nylon power connector (J6) on the controller board, as mentioned earlier. The connector at the free end of this cable should be a four pin shell, but with only 2 connector pins in place. Note that this connection is polarized to insure proper installation.

Next, locate the free end of the Disk Drive Power Cable that was connected to the floppy drive that was removed from the H/Z89 earlier, and connect it to the white nylon power connector on the hard disk drive unit. The Disk Drive Power Connector is not mounted to a circuit board, but rather it is embedded into the metal case of the hard disk drive. The Disk Drive Power Cable connected here should also have a four pin nylon connector shell, but all four pins on this connector must be present with four connecting wires colored red, orange, and black.

CAUTION! Improper installtion of these two power cables can result in permanent damage to the drive or controller when the power is turned on. Both of these connections are polarized to reduce the chances of such an accident. However, if you are uncertain about these connections don't hesitate to call SigmaSoft and Systems to ask for technical assistance.

Step #5, Final Assembly

Gently slide the hard disk drive unit all the way into the front of the H/Z89 or H/Z19 unit until the front bezel plate is seated properly. Mount the drive using the four #6 machine screws provided. Do not use screws longer than 1/4 inch for the two lower mounting holes on the side of the drive unit as they will likely twist off into the bracket. 3/8 inch machine screws can be used for the two mounting holes on the top of the drive unit.

Connect the free end of the Controller Interface Cable to the Disk Interface Connector on the Interface Board. For H8 systems this cable must be routed out the back of the cabinet and through an opening in the rear of the H8 to be connected to the Interface Board. The Hard Disk Interface connector on the Interface Board is the upper 34 pin connector for both the H/Z89 and H8 versions. The identical connector located below the Hard Disk Interface is the Interactive Graphics Controller Interface.

This completes the installation of the hard disk for internal mount systems. Apply power to the computer and test it for normal operation. Then proceed to the section on the Maintenance Software.

Centronics Printer Cable

The Universal Parallel Interface Board features 2 Centronics Parallel Ports, each of which can be used to drive a separate printer provided that they have a 36 pin Centronics type input. The two piece Centronics cable features an internal section, for connection to the H/Z89 backplate, and a longer external section for connection to the printer.

Begin by connecting the 10 and 12 pin connectors at one end of the internal cable to one set of the 10 and 12 pin connectors on the Interface Board. The 10 and 12 pin connector set closest to the CPU Logic Board should be used first, if they are not already being used.

Route the free end of the internal cable down and under the CPU and Terminal Logic Boards and to the backplate. Use the supplied mounting hardware to fasten the free end of the internal cable to the inside of the backplate. Any available DB-25 mounting hole can be used.

The external portion of the cable can then simply be connected between the outside of the backplate and the Centronics interface of the printer.

Atari Adapter Cable

The Atari Adapter Cable can be connected to either of the two 12 pin input connectors on the printer interfaces of the Universal Parallel Interface Board. The slotted side of the 12 pin connector should be positioned towards the CPU Logic Board. The free end of the cable can then be connected to any standard digital Atari or Wico trackball or joystick.

The standard Heath backplate does not provide a DB-9 mounting hole, so the cable will have to be simply routed out of an available opening. Note that replacement backplates are available which do provide DB-9 mounting holes.

Additional Hard and Floppy Disk Drives

The SigmaSoft Disk Systems feature the capability to add additional hard and floppy disk drive units. Up to three hard disk drives and four floppy drives are supported by the WD1002 controller, software, and SigmaROM. If you purchased an internal mount disk system, additional drives must be mounted into an external cabinet and connecting cables used between this cabinet and the WD1002 controller board which is located beside the original hard disk drive inside the H/Z89 unit. Both the cabinet and cables required to accomplish this are available from SigmaSoft and Systems.

If you purchased an externally mounted hard disk system, then you already have the extra cabinet space for a second drive in the external cabinet. SigmaSoft supplies each external mount hard disk system with a full height cabinet eventhough only a half height drive is used. This allows a second drive to be added above the first in this same cabinet.

To mount a second disk drive inside of the SigmaSoft drive cabinet, the first drive must be removed to replace the full height black plastic bezel plate with a half height plate. The replacement half height plate is normally supplied with each external mount system. It is located inside of the drive cabinet.

WARNING! During this installation proceedure, you will be handling the hard disk drive unit which is extremely sensitive to shock and vibration. These drives are typically rated by their manufacturer to withstand only 40 G's of shock without permanent damage. This amount of shock can be generated by dropping such a drive unit only a few inches onto a hard surface. Such a drop may trigger shock sensors inside of the drive unit which will void its warranty.

In addition to the spare bezel plate that is provided, an extra drive power cable is also present inside of the external drive cabinet. This spare cable can supply power to either a second hard or floppy disk drive.

The final step in installing additional drives is the connection of the required signal cables. A floppy disk drive only requires a single 34 conductor ribbon cable connected between it and the 34 pin floppy interface on the WD1002 controller. If you have multiple floppy drives to attach, a single cable must connect to each of them (daisy chain).

Hard disk drives also require a daisy chained 34 conductor ribbon cable as with the floppy drives. However, they also require a separate 20 conductor ribbon cable between the disk controller and each of the hard disk drive units involved. Note that there are three such connectors located on the disk controller, one for each possible drive unit.

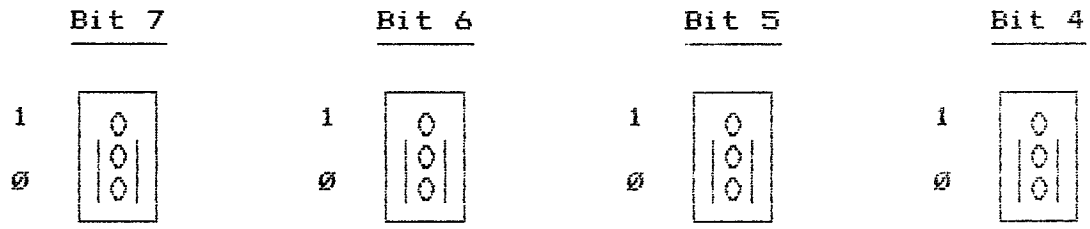
With all of these signal cable connections be sure to maintain the pin 1 orientations indicated on the circuit boards of the disk drives and the disk controller. The drive unit select jumpers and terminating resistor packs located on the drives must also be adjusted properly.

Port Address Selection Jumpers

The set of four jumpers in the lower right corner of the Universal Parallel Interface Board are the Port Address Selection Jumpers. Some older versions of the interface board also have a fifth jumper to the far right.

The positions of these jumpers determine the port address zone of the Universal Parallel I/O Board and all devices interfaced through it, including the hard/floppy disk controller, the Interactive Graphics Controller, and the two printer ports. The standard port address of Ø should be selected as shown below.

Port Address Selection Jumpers



Each of the four jumpers correspond to an address bit (A4 through A7), which together form a binary number which gives the first port address of the selected eight port address zone. The first four bits from the right (AØ through A3) determine the local ports (1 of 16) and so are considered to be zero when calculating the zone address. Remember that the calculated port address is only the first address of 16.

Unless your needs require a special port address, the port address setting illustrated above is recommended. If you must change the port address setting there are two important guidelines you must follow. The Universal Parallel Board must not be configured to operate at a port address that is currently being used by any other device connected to the H/Z89 or H8 computer, and there may be software changes that have to be made when the port address setting is changed.

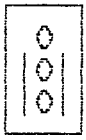
AC Line Voltage Configuration

All SigmaSoft products can be used with either the North American 12Ø Volt AC Line Power or the 24Ø Volt AC Line Power used in European countries. With Internal mount hard disk systems this adjustment is made with the existing line voltage switch on the bottom of the H/Z89 or H/Z19 cabinet. For the external disk cabinet this adjustment must be made by removing the drive cabinet's cover and repositioning a red plastic jumper that is located on the power supply circuit board. This jumper is labeled as a 12ØV/24ØV line voltage adjustment. Note that the 5ØHz line frequency used in European countries will not affect these disk systems.

The H8 CPU Board Type Jumper

The H8 version of the Universal Parallel Interface Board has an additional jumper located immediately beside the Hard Disk Interface Connector. The two positions of this jumper are labeled on the interface board as 2 and 4. The 2 position must be used if you are using an 8080 type CPU board in your H8 computer running at a system clock frequency of 2 MHz. The 4 position must be selected if you are using a Z80 type CPU board running at 4 MHz. If you are using a Z80 type CPU running at only 2 MHz, either position can be used.

H8 Interface CPU Jumper Settings



2 or 4 MHz Z80 CPU

2 MHz 8080 or Z80 CPU

Configuring the H/Z89 CPU Board for use with the SigmaROM

The installation of the SigmaROM on the H/Z89 CPU Logic Board alters some of the definitions of the DIP switch settings at SW501. If you have replaced the MTR-90 ROM on your CPU board with the SigmaROM, use the following chart to program this DIP switch.

SW501 Switch Definitions for use with the SigmaROM

Switch Sections 7 6 5 4 3 2 1 0	Boot Device	
0 0	A	H17 Controller Boot Enable
0 1	A	H47 Controller Boot Enable (Port 1740)
1 0	A	WD1002 Hard Disk Boot Enable
1 1	A	WD1002 Floppy Disk Boot Enable
0 0	B	H37 Controller Boot Enable
0 1	B	H47 Controller Boot Enable (Port 1700)
1 0	B	WD1002 Hard Disk Boot Enable
1 1	B	WD1002 Floppy Disk Boot Enable
0		Primary Boot Device is A (B is Secondary)
1		Primary Boot Device is B (A is Secondary)
0		Reserved (Must not be Selected)
1		Reserved (Must be Selected)
0		Console Baud Rate is 9600
1		Console Baud Rate is 19200
0		Normal Boot
1		Auto Boot on Power Up or Reset

Examples of the Most Common Settings

0	0	1	1	1	0	0	0	WD1002 Hard Disk, and H17 Controller
0	0	1	0	0	0	1	0	WD1002 Hard Disk, and H37 Controller
0	0	1	0	1	1	1	0	WD1002 Hard Disk, and WD1002 Floppy Disk

The following pages describe the various utilities that are provided on the Hard Disk Support Software Distribution Disks. These utilities are used to prepare and organize the hard disk for data storage.

Although it is impossible to cause any physical damage to a disk drive through improper use of these programs, large amounts of data can easily be lost if extreme care is not taken while using them. For this reason it is recommended that the user first make a trial run through all of these programs to become familiar with their use. Once you are confident as to their operation, you can start from scratch and begin uploading your data library.

HDFORMAT

The first step to use a hard disk drive after its installation is to format it for data storage. This is done by the HDFORMAT utility under either HDOS or CP/M. If you wish to use the hard disk for both HDOS and CP/M, you only need to format it under one of the operating systems, not both. Also, it does not matter which operating system you use to perform the format since the HDOS and CP/M versions of this utility have identical functions.

Under HDOS type:

```
>HDFORMAT
```

For CP/M type:

```
A>HDFORMAT
```

You will be asked for the port address and drive select values for the drive you have installed. These values are both zero (the defaults) unless you have installed multiple hard disk drives or have changed the setting of the Port Address Selection Jumpers on the Interface Board. The valid drive select values are Ø, 1 and 2.

If an error message is displayed here, it is because the HDFORMAT utility can not locate the hard disk drive at the port address and drive select you have specified. Be sure that the installation of the Interface Board, Controller Board, Hard Disk Drive, and the connecting cables is correct. Refer to the Configuration section of this manual for more information on these parameters.

A series of questions follow which must be answered according to the type of drive you have. The chart below summarizes. If you are uncertain about the type of drive you are using, locate the drive model number label on your system. With external systems, this small white label is on the back of the drive cabinet. With internal systems, the label is located on the back of the drive unit, near its power connector.

Summary of Hard Disk Drive Formatting Parameters

Mounting	External					Internal	
Manufacturer	Seagate					LaPine	
Platter Size	5.25 Inches					3.5 Inches	
Drive Height	Half	Half	Half	Full	Full	Half	Half
Model Number	ST213	ST225	ST251	ST4038	ST4051	T 10	T 20
Formatted MBytes	10.07	20.15	40.30	30.02	42.03	10.07	20.15
Number of Cylinders	615	615	820	733	733	615	615
Number of Heads	2	4	6	5	7	2	4
Parking Cylinder	620	620	820	733	733	615	615
Precompensation	256	256	0	256	256	0	0
Sectors per Track	32	32	32	32	32	32	32
Interleave Factor	18	18	18	18	18	18	18
Step Rate	.035	.035	.035	.035	.035	.035	.035

Finally, you will be asked if you wish to format the hard disk and erase it of all data. If you answer with a Yes, the formatting process will begin. A verify will also be performed to locate any possible bad sectors. This utility can be aborted at any time by typing Control-C.

Note that it is normal for even a new hard disk drive to have some bad sectors. However, if the number of bad sectors reported is excessive, contact SigmaSoft technical assistance immediately. The hard disk drive may have been damaged in shipment. Under HDOS bad sector numbers should be entered when the partition is initialized. Under CP/M this must be done by modifying the partition's directory using the FINDBAD utility that has been provided.

Once the format is complete, the utility will finish by creating special tables of information on the first cylinder of the hard disk drive. These tables contain format and partition data which are vital to the operation of the rest of the software in this package. Refer to the Customer Support section of this manual for more complete information on these tables.

In the event that the first of the format tables should become damaged, one of the duplicate copies will be used and the error will be reported on the screen with a single vertical broken bar character (¦). If one of these characters should ever appear, the user is advised to back up all of the data stored on the hard disk and reformat the drive to correct these tables in cylinder zero.

It is strongly recommended that this utility only be kept in a safe place between uses to minimize the risk of accidental use. The next required step in this software installation proceedure is to create data partitions for the operating systems of your choice. This is done with the HDPART utility.

Using HDPART

The HDPART utility is used to create and delete data partitions for the HDOS and CP/M operating systems. If you wish to use the hard disk for both HDOS and CP/M, you only need to partition it under one of the operating systems, not both. Also, it does not matter which operating system you use to perform the partition since the HDOS and CP/M versions of this utility have identical functions.

Under HDOS type:

```
>HDPART
```

For CP/M type:

```
A>HDPART
```

You will be asked for the port address and drive select values for the drive you have installed. These values are both zero (the defaults) unless you have installed multiple hard disk drives or have changed the setting of the Port Address Selection Jumpers on the Interface Board. The valid drive select values are Ø, 1 and 2.

If an error message is displayed here, it is because the HDPART utility can not locate the hard disk drive at the port address and drive select you have specified. Refer to the Configuration section of this manual for more information on these parameters.

This program requires the existance of a valid partition table on the hard disk. This table is created by the HDFORMAT utility. As with HDFORMAT, this utility can destroy large amounts of data stored on the hard disk and should only be used after all of the important files on the hard disk drive have been duplicated using another disk drive.

Editing the Partition Table

HDOS can not allow a single disk drive unit to be larger than 16 megabytes and for CP/M this limit is 8 megabytes. To correct this problem, HDPART allows the storage capacity of the physical drive to be divided into multiple logical drives called partitions. This technique also has the advantage that a large data library can be better organized by assigning a name to each partition that describes its contents or intended use.

Partitions are created by allocating a number of cylinders to a partition name for a particular operating system (HDOS or CP/M). The actual size of the cylinders and the count of cylinders available depends on the type of hard disk drive you have installed. However, this information will be displayed by HDPART to aid your decisions as to how the storage space should be allocated.

To add a partition, specify a type (HDOS or CP/M), the cylinder count (size) and a partition name. Free areas of the disk that are available for allocation will be indicated as such. This utility can be aborted at any time without altering the disk by typing Control-C.

If you do not need all of the available space, it is a good idea to leave some cylinders free for future use. Smaller partition sizes (1 to 2 megabytes) are also recommended since they are used more efficiently by the HDOS and CP/M operating systems for most applications.

HDPART will require that partition names be both valid and unique. Note that two partitions of the same name can be used if they are of differing types (HDOS and CP/M for example). HDPART will also not allow any partition to be created which exceeds the drive size limitations of a particular operating system. These size limits are 16 megabytes for HDOS and 8 megabytes for CP/M.

A valid partition name is defined as having less than 12 printable characters (no control characters), with only the comma character being excluded. Also, the first character of a partition name must be an alphabetic character (A through Z). Lower case alphabetic characters are considered to be equivalent to their upper case.

Selecting a Default Boot Partition

The final step in preparing a new partition table is selecting a default boot partition. This partition is indicated in the partition directory by an asterick symbol (*). Only one default boot partition can be selected at one time. The partition selected should be the system partition you will be booting from most often using the SigmaROM. It may in fact be your only bootable partition.

Normally the SigmaROM requires a partition type and name specification each time you boot the hard disk drive(s). However this will not be required for the selected default boot partition. Refer to the SigmaROM operation section of this manual for more information.

It is recommended that frequently booted partitions be placed as close as possible to the front of the partition directory for faster boot operations. Use the higher cylinder number areas for data partitions that will just be accessed after booting from other (system) partitions.

Installing a New Partition Table

Once the hard disk partition table is organized as you like, the next step is to write it back to the hard disk drive over the old version. This is done by simply exiting the HDPART utility and responding with 'YES' to the confirmation prompt.

CAUTION! If you have deleted any partitions during a partition table editing session with HDPART, all of the data that may have been present in those partitions will be erased. These partitions can be saved by aborting HDPART with a 'NO' at the confirmation prompt.

Under CP/M, new partitions can simply be mounted by the ASSIGN.COM utility that has been provided. However, new HDOS partitions must be initialized by the standard INIT.ABS utility before they can be used.

Using HDPARK

The HDPARK utility is used to park the recording heads of the hard disk drive to prepare it for shipment. Most types of hard disk drives feature a special cylinder of the disk called a parking area. The parking area does not have a recording surface that can be damaged if the drive unit were to experience excessive amounts of shock or vibration. Since this is always a serious possibility when a hard disk is transported, the HDPARK utility should be used to minimize the risk.

For HDOS type:

```
>HDPARK
```

Under CP/M type:

```
A>HDPARK
```

You will be asked for the port address value for the drive you have installed. This value is zero (the default) unless you have installed multiple hard disk drives or have changed the setting of the Port Address Selection Jumpers on the Interface Board. The HDPARK utility will automatically locate all of the hard disk drives at the specified port address and park them simultaneously.

If an error message is displayed here, it is because the HDPARK utility can not locate any hard disk drives at the port address you have specified. Refer to the Configuration section of this manual for more information on this parameter.

Once the recording heads are parked, a message will be displayed to this effect. All currently mounted drives under HDOS will be dismounted. When you see this message, immediately turn the power switch to the hard disk drive unit off.

If you allow the program to exit before removing power from the drive, the heads will likely be unparked by the next disk access. Turning the power switch to the drive back on will also unpark the heads. There is a characteristic stepper motor sound when the heads unpark.

Hard disk drives are always shipped from the manufacturer in a parked state and the same should be done by the user if it should ever become necesary to return the drive to SigmaSoft for servicing.

Introduction

The Loadd utility is used to install SigmaSoft device drivers into a CP/M 80 system. No such program is needed under the HDOS system. This utility dynamically allocates space from the Transient Program Area of the CP/M system and reserves it for the installed driver module. The principal advantages of this utility over running the SigmaBIOS is ease of installation and compatiblity with all CP/M 80 systems. The disadvantage of using this utility is that it is not as memory efficient as running SigmaBIOS although it is required to transport SigmaBIOS to a new CP/M system. Furthermore, SigmaBIOS is required to boot disk drives interfaced through the WD1002 controller.

The CP/M user has the option of either running the SigmaSoft disk system through the supplied device drivers on a permanent basis, or creating a bootable SigmaBIOS disk which requires the device drivers only initially. Remember that with the device driver approach your system must be booted on an existing disk system before the SigmaSoft disks can be used. However, once a bootable SigmaBIOS disk has been created, this limitation is eliminated if you are using Heath CP/M.

Theory

The Loadd utility begins by reading the specified driver file into memory and testing the code for validity. If the file does contain a valid driver then a search of the CP/M system is made to locate a possible matching driver which has already been loaded. If a matching driver is found, then the Loadd utility will request the resident driver to unload, so that the new version may be loaded in its place. Only if the resident driver responds to the unload request will the reload occur. This is to provide the capability to reload a driver which may have had set changes made while at the same time protect drivers which may be processing interrupts.

If a matching driver is not already present in the system, the user will be prompted for a location to load the new driver. This location can either be 2048 bytes below the BDOS (top of the TPA), or above the system BIOS. This second option assumes that 64k of memory is installed in the computer and that the BIOS has been moved down to make room for the device driver module.

The Load Utility then uses a relocation table at the end of the device driver file to modify the driver code so that it will execute at the calculated load address. The modified driver code is then moved into place at the load address and called to sign on.

If the driver is requested to load below the CCP, two important patches are made to the CP/M system to reserve this memory area. The first is to the BDOS pointer in the System Parameter Area and the second is to the portion of the warm boot code in the BIOS which initializes this pointer.

Loading Device Driver Modules

Before any of the functions or features of a device driver can operate, the device driver must first be loaded into the CP/M system from the corresponding driver file using the Loadd utility. Examples of the syntax for doing this are:

```
A>LOADD HDC:

A>LOADD HDC: LOW

A>LOADD UPC: HIGH
```

The proper driver name to type following the Loadd command will depend on the particular device driver you wish to load. Note that the driver file name specified to load must have the DVD device driver file name extension which is the default.

The load utility will display a table of all of the currently loaded device driver modules showing their names, sizes, and load locations. The load locations can either be below the CCP (the default) or above the system BIOS. If this is the first time this driver has been loaded you will be asked if there is space available above the BIOS. If not, simply hit return and the driver will be loaded below the CCP. Note that the Low/High designation can also be made on the command line as shown in the examples above.

Once loaded, the driver will be operational and will remain locked into the CP/M system until the next cold boot so that it need not be reloaded. Most drivers can be reloaded without rebooting so that set changes will take immediate effect. If a driver can not be reloaded, an appropriate error message will be displayed.

Multiple drivers of different names can be loaded simultaneously into the CP/M system. However, if the drivers conflict, (such as two printer drivers of different names configured for the same printer) only the last driver loaded will be active for that device.

Allocating Space Above the BIOS

The standard technique of installing device drivers below the CCP has two drawbacks. First, the CCP is locked into place removing 2k bytes of memory from the system. Second, installing drivers below the CCP is somewhat BIOS version dependent and so may not be possible with some non-standard CP/M implementations. If this is the case with the CP/M system you are using, a BIOS Incompatibility Error message will be displayed when you attempt to load a driver below the CCP.

Allocating space for a driver above the BIOS is a simple process which eliminates these problems. First, attempt to load the driver below the CCP so that the load utility will show you the size of the driver. This size specification is given in bytes and must be converted to a kilobyte count for the MOVCPM utility. Round the size given up to the nearest multiple of 1024 and drop the three right digits to convert the number to a kilobyte value as shown in the chart below.

Byte Size to Kilobyte Size Conversion Chart

Size in Bytes	Kilobyte Size	System Size
1 through 1024	1	63
1025 through 2048	2	62
2049 through 3072	3	61
3073 through 4096	4	60
4097 through 5120	5	59
5121 through 6144	6	58
6145 through 7168	7	57
7169 through 8192	8	56
8193 through 9216	9	55
9217 through 10240	10	54
10241 through 11264	11	53
11265 through 12288	12	52
12289 through 13312	13	51
13313 through 14336	14	50
14337 through 15360	15	49
15361 through 16384	16	48

Run the MOVCPM utility supplied with your CP/M software and specify the system size to be 64k minus the kilobyte size as shown in the above chart. For example, the WDC: driver is less than 4096 bytes in size but larger than 3072 so the command line would be:

```
A>MOVCPM 60
```

The MOVCPM utility will create the new CP/M system in memory only. Use your CP/M SYSGEN utility to copy it to a disk. Type:

```
A>SYSGEN
```

Note that the names of the MOVCPM and SYSGEN utility may vary depending on the type of CP/M system you are using.

Driver Loading Errors

The process of loading a device driver is successful as long as an error message was not printed. If any error message appears then the driver will not be active and none of the functions of that driver can be used until a successful load operation is completed.

Introduction

The Assign utility is provided under both HDOS and CP/M for the purpose of mounting and dismounting hard disk drive partitions. These partitions must have first been created using the HDPART utility, and under HDOS they must also have been initialized.

Assign requires a partition name to perform a drive assignment, and only the names of partition types that match the currently booted operating system will be accepted. If no partition names are known by the user, a question mark can be specified instead, which will cause Assign to display the available partition directory. Assign also allows multiple partition assignments to be made on a single command line by separating them with commas. Below are some examples under HDOS:

```
>ASSIGN ?
>ASSIGN HDØ:=NAME
>ASSIGN HDØ:=NAME1, HD1:=NAME2, HD2:=NAME3
```

Examples under CP/M:

```
A>ASSIGN ?
A>ASSIGN B:=NAME
A>ASSIGN A:=NAME1, B:=NAME2, C:=NAME3
```

The Assign utility will automatically load the appropriate hard disk device driver if it has not already been done. Under CP/M the user may be prompted about space being available above the BIOS. If you are unfamiliar with this, simply hit return. Refer to the section on the LOADD.COM utility for a complete explanation. The Low and High designations of the Loadd utility can also be placed on the Assign command line under CP/M.

The Assign utility can also be used to dismount any hard disk partition so that it may be reassigned to another unit. This is an important feature since the number of available partitions can exceed the limits of mountable partitions under HDOS and CP/M. HDOS can only allow up to 8 partitions to be mounted at a single time and under CP/M this limit is 4. Some examples under HDOS are:

```
>ASSIGN HDØ:
>ASSIGN HDØ:, HD1:, HD2:
>ASSIGN SY1:, SYØ:=NAME, ?
```

Under CP/M type:

```
A>ASSIGN B:
A>ASSIGN A:, B:, C:
A>ASSIGN B:, A:=NAME, ?
```

Another important feature of the Assign utility under CP/M is its ability to automatically reassign disk units that have been replaced by hard disk partition assignments. For example, if you boot a floppy disk and then assign a hard disk partition to unit A:, the original unit A: (the booted floppy disk) will automatically be reassigned to the first available drive unit so that it can still be used. This condition can also be reversed by deassigning the hard disk partition from that unit.

Finally, Assign supports the simultaneous use of multiple hard disk drives by specifying a drive select value before the partition name. For example, to mount a different partition from three separate hard disk drives under HDOS type:

```
>ASSIGN SY0:=1 SYSTEM, SY1:=2 DATA, SY2:3 RECORDS
```

Under CP/M type:

```
A>ASSIGN A:=1 SYSTEM, B:=2 DATA, C:=3 RECORDS
```

The MAKESBC Utility

MakeSBC is a utility that will re-create the Software Boot Code portion of the format tables on cylinder zero of an installed hard disk. Normally this type of operation would have to be done by the HDFORMAT utility which requires that all data on the drive be moved to another system to save that information. MakeSBC elliminates the need to do this since it does not affect the partition information tables on a drive. This utility may be required if you change versions of the SigmaSoft Disk System support software and do not wish to re-format your drive. MakeSBC can also be used to correct some types of damage to the format of a hard disk should it ever occur.

The proceedure for using MakeSBC is quite simple. Just specify the port address and drive select values of your hard disk drive, when prompted for this information. The SBC will then be written onto the specified hard disk.

Public Domain Software

A number of public domain utilities are provided on the SigmaSoft disk system distribution disks to aid in using a hard disk drive. These programs are either self-documenting or have documentation files on the disk that explain their use. Since these utilities are not products of SigmaSoft and Systems they are not as thoroghly supported as our other products. These utilities may require modifications to be used with your particular system.

Introduction

The disk device drivers are mass storage device interfaces for the HDOS and CP/M operating systems. These drivers support virtually any hard or floppy disk drive through the Western Digital WD1ØØ2 controller. The HD.DVD and FD.DVD files are the HDOS versions of the hard and floppy device drivers respectively. These drivers function as standard HDOS directory type device drivers.

The HDC.DVD file is the CP/M version of the hard disk device driver. The WDC.DVD file is a combined hard/floppy device driver for CP/M. Combining these two functions under CP/M is necessary to minimize memory usage.

Performing a Set Operation

The Set utilities (Set.ABS under HDOS and Set.COM under CP/M) allow the user to configure various options available for a device driver. The Set utilities modify the driver by making patches in the code of the program and then writting the patched driver back to the device driver disk file, so that the change need not be made again. These disk device drivers support several of these options and they must be set properly for the driver to operate. An example of the syntax under HDOS would be:

```
>Set HD: Help
```

Under CP/M type:

```
A>Set HDC: Help
```

The values specified for a set operation may be given in several number bases by supplying the proper radix where decimal is the default. Each time a set operation is performed the set status table for all of the options will be displayed to verify that the desired change has been made.

The Help Option

The Help option will display the set status of all of the options to the system console without making any set changes to the driver. All of the values displayed will be in decimal, regardless of the number base they were originally set in.

The Port Option

The Port set option defines the I/O port address of the WD1ØØ2 Controller Board. The port address value set here must correspond to the port address selected on the interface board. The standard port address for this device is Ø.

The Step Option

The Step set option defines the track to track stepping speed for the FD: and WDC: floppy device drivers. This option is not needed for the hard disk drivers. This value depends on the capabilities of the floppy disk drives you are using. All integer step rates between 40 and 1 milliseconds are valid. Most floppy disk drives can operate at least as fast as 20 milliseconds per step, and some can step as fast as 3 milliseconds. If you experience excessive floppy disk retries or errors a higher step rate value should be used.

The Unit Option

The Unit set option defines the first drive unit that is not being used by the running CP/M BIOS. This option is not needed for the HDOS versions of the disk drivers. This option allows the user to control which drive select units will be used by CP/M to access the disk device drivers. For example, if the WDC: driver is set to Unit G:, then G: will be the first drive unit letter of the SigmaSoft floppy disk controller. The actual drive select units used for the SigmaSoft hard disk drives is determined with the Assign utility.

Set Option Summary for HD: and HDC:

Help	Print Set Option Summary With Status
Port x	WD Controller Port Address (0 Standard)
Unit x:	First Drive Unit for the WD1002 Controller

Set Option Summary for FD: and WDC:

Help	Print Set Option Summary With Status
Port x	WD Controller Port Address (0 Standard)
Step x	Floppy Disk Step Rate (20 Standard)
Unit x:	First Drive Unit for the WD1002 Controller

Loading Device Drivers

Under CP/M device drivers must be loaded into the system before use. Floppy disk drivers should be loaded using the LOADD.COM utility provided. HDOS device drivers will load automatically when mounted. Note that HDOS versions of the disk drivers also require an initialized disk. This can be done by using the INIT.ABS utility provided with the HDOS system to initialize either floppy disks or hard disk partitions by their names. To load an initialized device under HDOS type:

```
>MOUNT FD:
```

Under CP/M type:

```
A>LOADD HDC:
```

If you get an error, it will most likely be because either the FD.DVD (HDOS) or WDC.DVD (CP/M) file is not present on the system disk. Error messages should be self explanatory.

Note that you may be prompted about space being available above the BIOS with CP/M. If you are unfamiliar with this, simply hit return. Refer to the section on the LOADD.COM utility for a complete explanation.

Assigning Hard Disk Partitions

Hard disk device drivers under HDOS or CP/M must have at least one partition assigned for use by the ASSIGN utility. This utility will perform the device driver load operation automatically. The basic syntax under HDOS is:

```
>ASSIGN HD:=NAME
```

For CP/M type:

```
A>ASSIGN H:=NAME
```

In these examples 'NAME' must be an existing partition name as created using the HDPART utility. If you are not certain what partition names are available, they can be displayed under HDOS by typing:

```
>ASSIGN ?
```

For CP/M type:

```
A>ASSIGN ?
```

For further information, refer to the section of this manual that deals with the ASSIGN utility.

Copying files to and from the Hard Disk

Under HDOS these device drivers functions in just the same way as the SY0: and the DK0: devices. With CP/M they will become standard CP/M device units A: through P: (H: in the above example) For HDOS type:

```
>CAT HD:
```

Under CP/M type:

```
A>DIR H:
```

Any copy utility such as PIP can be used to transfer files to and from the hard and floppy disks. An example of this under HDOS is as follows:

```
>PIP HD:=PIP.ABS
```

For CP/M type:

```
A>PIP H:=PIP.COM
```

These disk devices can also be sysgened as bootable devices using the SYSGEN.ABS and BOOT.ABS utilities provided with HDOS or the MOVCPM and SYSGEN.COM utilities provided with CP/M. Refer to the section of this manual dealing with the installation of the SigmaBIOS software for an explanation of the later.

Hard Disk Space Usage

On a high capacity hard disk system it is very important to understand that the file sizes that are normally displayed in a HDOS or CP/M file directory may not accurately portray the amount of disk space that those files are really using. To show the total disk space used by a file under HDOS type:

```
>CAT/ALL
```

Under CP/M type:

```
A>STAT *.*
```

Introduction

The UP:/UPC: Universal Parallel printer device driver is a general purpose printer driver for both HDOS and CP/M. It is compatible with virtually any type of printer and parllel printer interface.

UP:/UPC: supports the entire ASCII character set. All printable and non-printable control characters will be passed to the printer with the parity bit intact. This is to prevent interference with any of the special features of a printer that the user may wish to access by passing control codes.

Performing a Set Operation

The Set utilities (Set.ABS under HDOS and Set.COM under CP/M) allow the user to configure various options available for a device driver. The Set utilities modify the driver by making patches in the code of the program and then writting the patched driver back to the device driver disk file, so that the change need not be made again. The UP: and UPC: device drivers support many of these set options. An example of the syntax under HDOS would be:

```
>Set UP: Help
```

Under CP/M type:

```
A>Set UPC: Help
```

Although most of these set options are optional, several control the manner in which the driver communicates with the printer. These options must be set properly for the driver to operate.

The values specified for a set operation may be given in several number bases by supplying the proper radix where decimal is the default. Each time a set operation is performed the set status table for all of the options will be displayed to verify that the desired change has been made.

The Help Option

The Help option will display the set status of all of the options to the system console without making any set changes to the driver. All of the values displayed will be in decimal, regardless of the number base they were originally set in.

The Form and NoForm Options

The Form and NoForm set options set and reset the form flag. If this flag is set the printer will advance to the top of the next unused form when the driver is closed after a print operation.

The Skip and NoSkip Options

The Skip and NoSkip set options set and reset the skip flag. If this flag is set, the driver will skip all redundant form feeds. If nothing has yet been printed on a form, then the driver will ignore any form feeds that might occur, which would normally cause forms to be skipped blank. This feature can be very useful while printing a file that has already been paged with form feed characters.

The PPI and NoPPI Options

The PPI and NoPPI set options set and reset the PPI (8255 type Programmable Peripheral Interface) flag. This option is not available with serial versions of the UP: and UPC: drivers.

This flag should only be set if you are using the Heath/Zenith Multifunction I/O Card (Z-89-11) or a similar board to interface your printer. This flag must not be set (NoPPI) if you are using one of the Centronics interfaces on the SigmaSoft Universal Parallel Interface Board.

The Page Option

The Page set option determines the count of lines per page that will be printed before skiping the form perforation. Also, note that zero can be set as the lines per page count to effectively disable paging.

The Port Option

The Port set option defines the I/O port address of the printer devices. The port address value set here must correspond to the port address values of the particular interface board being used. The standard port address of the first Centronics interface on the Universal Parallel I/O Board is 15. The standard serial printer port address of the H/Z89 is 224 decimal (340 octal).

The Ready Option

The Ready set option is for use in configuring the handshaking of the driver with the printer through a Centronics parallel interface.

When using the SigmaSoft Universal Parallel Interface with a standard Centronics cable, these values should be set to 30, 24. If you are instead using an 8255 type Programmable Peripheral Interface (such as the Heath/Zenith Multifunction I/O Card or a similar board) to interface your printer, these values should be 128, 128.

The first value is used as a Boolean And mask to selectively clear bits that are to be ignored in the input status byte. The second value is then used as the binary compare pattern to determine if the printer is ready to receive the next data byte.

A full Centronics interface will have four or five bits which collectively indicate the printer status (Busy, error, paper out, etc.). This system allows the user to configure the device handshaking to monitor any or all of the condition bits of the input status byte. Refer to the chart below for an example of calculating the Ready set values for a particular system.

Ready Set Option Values Calculation Example

Bit	Value	Ready Pattern	Indicates
Ø	1	–	Data Acknowledge
1	2	Ø	Printer Not Busy
2	4	Ø	Paper Not Empty
3	8	1	Device Selected
4	16	1	No Printer Error
5	32	–	Undefined
6	64	–	Undefined
7	128	–	Undefined

Bits 1,2,3, and 4 should be monitored, so And mask would be ØØØ1111Ø binary (3Ø decimal) to mask all other bits of status byte clear. The logical And result is then compared to the ready value (second set option value) which would be ØØØ11ØØØ binary (24 decimal).

The Init Option

The Init set option determines the 16 byte printer initialization sequence which is output to the printer device each time a print operation is performed.

This data should contain any of the control characters or escape sequences that are required by your printer to initialize. This option can also be used to configure the printer for any special default modes that are desired. Refer to the operations manual for your printer to determine what modes are available. The following chart list the recommended values for this option for several different printer types. All unused values of this sequence should be set to zero.

Recommended Values for the Init Option

Values	Printer Type
27,64	Epson/Star Gemini/Panasonic/Riteman
17	IDS/C. ITOH/Okidata

Set Option Summary for UP: and UPC:

Help	Print Set Option Summary With Status
Form	Form Feed Printer After a Print Command
NoForm	No Form Feed After a Print Command
Skip	Skip Redundant Form Feeds
NoSkip	Pass all Form Feeds
PPI	Printer Interface is 8255 Type PPI
NoPPI	Printer Interface is SigmaSoft Type Centronics
Page x	Count of Lines per Page
Port x	Printer Port Address (8 or 224 Standard)
Ready x,x	Printer Device Handshaking (30, 24 Standard)
Init x,x,x,...	16 Byte Printer Initialization Sequence

Loading the Device Driver

Under CP/M the UPC: driver must be loaded into the system using the LOADD.COM utility provided. The UP: driver under HDOS will load automatically when used. To manually load the driver under HDOS type:

```
>LOAD UP:
```

Under CP/M type:

```
A>LOADD UPC:
```

If you get an error, it will most likely be because either the UP.DVD (HDOS) or UPC.DVD (CP/M) file is not present on the system disk. Error messages should be self explanatory.

Note that you may be prompted about space being available above the BIOS with CP/M. If you are unfamiliar with this, simply hit return. Refer to the section on the LOADD.COM utility for a complete explanation of this.

Printing Text Files

Under HDOS the UP: driver is a direct replacement for the standard LP: device. With CP/M the UPC: driver replaces the standard printer routine in the BIOS and becomes the system list device (LST:). This insures compatibility with application software that uses these standard devices for printer output.

ASCII text files can be output to the printer using the UP:/UPC: driver with the standard PIP utility. For HDOS type:

```
>PIP UP:=DEMO.TXT
```

For CP/M type:

```
A>PIP LST:=DEMO.TXT,EOF:
```

Introduction

SigmaBIOS is a BIOS (Basic Input and Output System) replacement for the standard Heath CP/M on the H/Z89 computer. This software in conjunction with the SigmaROM allows the user to create and boot both hard disk partitions and floppy disks under the CP/M operating system.

All of the capabilities of the original Heath CP/M BIOS remain intact except for the Z67 disk support which is considered obsolete. Many new features have been added such as support for the WD1002 disk controller, parallel printer I/O, and more thorough support for the H17 disk controller.

Installing SigmaBIOS

Sysgening a new system disk with SigmaBIOS requires the proper SigmaBIOS file and several important utility programs. Some of these files are provided on the SigmaSoft Hard Disk Support Disk (CP/M version) while others must be copied from your original Heath CP/M distribution disks. Refer to the chart below for a complete list of the required files.

Summary of Files Required to Create a Bootable SigmaBIOS Disk

Name of Required File	Supplier
ASSIGN.COM	SigmaSoft
HDC.DVD (or WDC.DVD)	SigmaSoft
MOVCPM.COM	SigmaSoft
SBIOS?.SYS	SigmaSoft
MOVCPM??.COM	Heath
SYSGEN.COM	Heath
PIP.COM	Heath

Begin by selecting the proper files for your intended destination disk and copy them to a disk which can be booted on one of your existing disk controllers. Note that the exact names of the SBIOS?.SYS and MOVCPM??.COM files depend on your particular system. Refer to the charts below for listings of the available files.

The disk that is to be sysgened with SigmaBIOS is the destination disk. The type of disk controller you wish the new system disk to boot on determines the version of the MOVCPM program that you must use. The MOVCPM.COM file is provided by SigmaSoft and is for sysgening disks that will be booted on either the SigmaSoft disk system, or the Heath H17 controller. The other versions shown are provided by the Heath Company and are for sysgening a SigmaBIOS disk that will boot on one of their disk controllers. Note that even if you are using the SigmaSoft MOVCPM utility you must still have one of the Heath versions on your system disk since they are required by MOVCPM to operate.

Summary of Available Sysgen Destinations

Program Name	Destination Disk Controller	Provided by
MOVCPM.COM	WD1002 Hard Disk	SigmaSoft
MOVCPM.COM	WD1002 Floppy Disk	SigmaSoft
MOVCPM.COM	H17 (80 Track or Double Sided)	SigmaSoft
MOVCPM17.COM	Heath Hard Sectored H17	Heath
MOVCPM37.COM	Heath Soft Sectored H37	Heath
MOVCPM47.COM	Heath Eight Inch H47	Heath

Refer to the chart below to select the proper SBIOS?.SYS file for your system. If you wish the system on the destination disk to be able to read and write to all of the different types of disk controllers available in your system, you must use the supplied SBIOS file that supports all of the proper controller types. The supplied DD.COM utility can be used to compare their sizes, which relates to the amount of user memory your system will have with the new SBIOS. The WD1002 indicates that both the SigmaSoft hard and floppy disk systems are supported.

BIOS File Name Summary

File Name	Supported Disk Controllers
SBIOS1.SYS	WD1002 Only
SBIOS2.SYS	WD1002, and Heath H17
SBIOS3.SYS	WD1002, and Heath H37
SBIOS4.SYS	WD1002, and Heath H47
SBIOS5.SYS	WD1002, Heath H17, and H37
SBIOS6.SYS	WD1002, Heath H37, and H47
SBIOS7.SYS	WD1002, Heath H47, and H17

Once all of the proper files are gathered onto a booted CP/M disk, the user must then mount the desired destination for the new system. This of course requires that the destination disk be formatted. If the destination is a hard disk, then the desired hard disk partition must also be assigned (refer to the ASSIGN.COM utility documentation).

The following example will illustrate the process of sysgening a hard disk partition with the SigmaBIOS version that also supports the Heath H17 controller (SBIOS2.SYS). If you wish to sysgen a different type of disk, or use a different version of the SigmaBIOS, the file names shown below must be adjusted accordingly.

```
A>ASSIGN H:=PARTNAME

A>MOVCPM * SBIOS2.SYS
```

Remember that MOVCPM.COM requires that either MOVCPM17.COM, MOVCPM37.COM, or MOVCPM47.COM be present on your system disk. MOVCPM will ask for the type of destination disk you wish to sysgen, WD1002 hard disk, WD1002 floppy disk, or H17 floppy disk (with 80 track and double sided capability). This selection must be appropriate for the type of disk drive you have installed at the drive unit given to the SYSGEN utility in the following step. Type:

```
A>SYSGEN
```

When SYSGEN asks for a source drive name, simply hit the return key to skip this question since the new system will have already been placed into memory by the MOVCPM utility. SYSGEN will then ask for a destination drive, and you should enter the drive letter for the new disk you have mounted to be sysgened (H: in the example above). Type an extra return to exit the SYSGEN program.

The final step is to copy the new SBIOS file to the destination disk with the PIP utility (changing the name of the file in the process) as follows:

```
A>PIP H:BIOS.SYS=SBIOS2.SYS[O]
```

Be sure that the same SBIOS?.SYS file is used for the PIP command as was used with the MOVCPM operation. Also, be sure that the SBIOS?.SYS file is renamed on the destination disk to BIOS.SYS. For a more complete explanation of the functions of the MOVCPM.COM and SYSGEN.COM utilities refer to your Heath CP/M Users Manual.

The CONFIG Utility

The SigmaSoft Disk System includes a new configuration utility named CONFIG.COM for use with the SigmaBIOS that replaces the Heath CONFIGUR.COM utility. This utility is used to define all of the various operating parameters of the SigmaBIOS. CONFIG is completely self-documenting. However, if you are unfamiliar with this program you should refer to your Heath CP/M Users Manual.

When SigmaBIOS is booted for the first time on a new system, some of the facilities of that system may not operate properly until they are configured properly with the CONFIG utility. For example, if you are using a terminal baud rate other than 9600, the console I/O will not operate when the system is booted until corrected with CONFIG. The following console escape sequence will temporarily correct the problem so that the CONFIG utility can be run.

Temporary Baud Rate Correction Sequence

Be sure the CAPS LOCK key is up.
Press the Off Line key.
Press the ESC key.
Press the r key.
Press the SHIFT and L keys together.
Press the Off Line key again.

Drive Select Unit Organization

Each time the SigmaBIOS is booted, it organizes all of the available disk drive units according to a predefined order. Each of these drive units are then assigned to a particular drive select unit letter (A: through P:) for access by the user. A fixed number of units will be reserved for each type of disk controller that is installed into your system. The chart below lists these fixed unit sizes and their priority.

Device Unit Sizes for the SigmaBIOS Disk Controller Types

Priority	Disk Controller Type	Number of Units
First	The Booted Device	3 or 4
Second	Heath H17 Floppy Disk	3
Third	Heath H47 Floppy Disk	3
Fourth	Heath H37 Floppy Disk	3
Sixth	SigmaSoft WD1002 Floppy Disk	3

The booted disk controller will always be assigned first, followed by the rest of the controller types that are supported by the particular SBIOS?.SYS in use.

For example, if you boot a SigmaBIOS system that only supports the WD1002 controller and the Heath H37 controller from a hard disk partition, units A:, B:, C:, and D: would be reserved for the four hard disk partitions. Units E:, F:, and G: would be reserved for the three H37 floppy drives. No units would be reserved for the H17 floppy drives because the SBIOS being used does not support it (in this example). Units H:, I:, J:, and K: would then be assigned to the four WD1002 floppy drives. Notice that the four units of the WD1002 hard disk controller were also skipped since it was the booted controller in this example.

Introduction

The SigmaROM is a Central Processing Unit (CPU) monitor replacement for the H/Z89. The SigmaROM supports all of the same features of the Heath MTR-90 ROM except for booting capabilities for the Heath Z67 eight inch hard disk system, which is now considered to be obsolete. Instead, the SigmaROM provides full booting capabilities for the SigmaSoft hard and floppy disk system. However, it is important to stress that the SigmaROM is not required to use any of the SigmaSoft disk systems, only to cold boot them. Since most of the functions of the SigmaROM are identical to those of the MTR-90 ROM, only the new functions will be described here.

Configuration

Before the SigmaROM can be used to boot the SigmaSoft disk system, it must be properly configured for the particular types of disk controllers you are using. For complete information on this, refer to the Configuration section of this manual.

The SigmaROM can only allow two disk controllers to be configured as boot devices at any one time. Remember that this does not limit the total number of disk controllers that can be used, just the number that can be booted. One of these two boot devices must be designated as the primary boot device while the other will become the secondary device. Refer to the chart below for a summary of all 20 of the available combinations.

Supported SigmaROM Boot Device Configurations

Primary Boot Device	Secondary Boot Device
SigmaSoft WD1002 Hard Disk	SigmaSoft WD1002 Floppy Disk
SigmaSoft WD1002 Hard Disk	Heath H17 Hard Sectored Floppy
SigmaSoft WD1002 Hard Disk	Heath H37 Soft Sectored Floppy
SigmaSoft WD1002 Hard Disk	Heath H47 Eight Inch Floppy
SigmaSoft WD1002 Floppy Disk	SigmaSoft WD1002 Hard Disk
SigmaSoft WD1002 Floppy Disk	Heath H17 Hard Sectored Floppy
SigmaSoft WD1002 Floppy Disk	Heath H37 Soft Sectored Floppy
SigmaSoft WD1002 Floppy Disk	Heath H47 Eight Inch Floppy
Heath H17 Hard Sectored Floppy	SigmaSoft WD1002 Hard Disk
Heath H17 Hard Sectored Floppy	SigmaSoft WD1002 Floppy Disk
Heath H17 Hard Sectored Floppy	Heath H37 Soft Sectored Floppy
Heath H17 Hard Sectored Floppy	Heath H47 Eight Inch Floppy
Heath H37 Soft Sectored Floppy	SigmaSoft WD1002 Hard Disk
Heath H37 Soft Sectored Floppy	SigmaSoft WD1002 Floppy Disk
Heath H37 Soft Sectored Floppy	Heath H17 Hard Sectored Floppy
Heath H37 Soft Sectored Floppy	Heath H47 Eight Inch Floppy
Heath H47 Eight Inch Floppy	SigmaSoft WD1002 Hard Disk
Heath H47 Eight Inch Floppy	SigmaSoft WD1002 Floppy Disk
Heath H47 Eight Inch Floppy	Heath H17 Hard Sectored Floppy
Heath H47 Eight Inch Floppy	Heath H37 Soft Sectored Floppy

Command Set

Each time the H/Z89 computer is turned on, or the Master Reset function is performed (by simultaneously pressing the RESET and the right hand SHIFT keys), the SigmaROM will display a message showing the version number of the ROM to confirm that the computer is operational. The SigmaROM will also clear the screen and sound an audible beep.

The SigmaROM will then display a prompt (S:) indicating that it is ready to accept a command. The chart below summarizes the available commands of the SigmaROM. For a complete description of these commands, refer to your Heath documentation on the MTR-90 ROM.

Summary of SigmaROM Command Set

Boot
Convert
Go
In
Out
Program Counter
Radix
Substitute
Test
View

Booting a Hard Disk Partition

The most important feature of the SigmaROM is its ability to boot the SigmaSoft WD1002 hard and floppy disk controller. However, the WD1002 controller must be selected as either the primary or secondary boot device before this is possible. Refer to the chart above and to the Configuration section of this manual to insure that this configuration has been made.

The basic syntax of a boot command is the character 'B' optionally followed by an 'S' to indicate that the desired device is connected to the secondary boot disk controller. This can then be followed by either a '1' or '2' character to indicate the proper drive select unit, if it is not drive select unit zero (the default). Some examples follow:

Examples of Booting a Floppy or Default Hard Disk Partition

Syntax	Boot Controller	Drive Select Unit
S: Boot	Primary Device	Zero
S: Boot1	Primary Device	One
S: Boot2	Primary Device	Two
S: Boot SD	Secondary Device	Zero
S: Boot SD1	Secondary Device	One
S: Boot SD2	Secondary Device	Two

If you are booting a hard disk partition, the SigmaROM will attempt to boot the default partition at the drive select unit you have specified. If you do not wish to boot the default partition, or if a default boot partition has not been defined with the HDPART utility, you must supply a partition type and name after the boot command. Some examples are:

Examples of Booting a Hard Disk Partition by Name

Syntax	Function Performed
S: Boot:HDOS, PARTNAME	Boots PARTNAME on first drive
S: Boot1:CPM, ARCHIVES	Boots SYSTEM on second drive
S: Boot2:HDOS, RECORDS	Boots RECORDS on third drive
S: Boot SD:CPM, BASIC	Boots BASIC on first drive
S: Boot SD1:HDOS, GAMES	Boots GAMES on second drive
S: Boot SD2:CPM, SYSTEM	Boots SYSTEM on third drive

Note that a colon character must proceed the partition type specification and a comma character must proceed the partition name specification. Either lower or upper case alphabetic characters may be used. The BACK SPACE and DELETE keys will provide some editing capabilities.

The SigmaROM will assume the standard I/O port address of the Universal Parallel Interface Board, which is Ø. If you have changed this configuration on the interface board, the Boot command must be proceeded by a Substitute command to patch in the correct port address. The address to patch in the port address at is Ø4ØØ74 split octal or 2Ø3C Hexadecimal.

The following section is provided to aid those who wish to build their own cables for driving printers, graphics input devices, or any other device that can be interfaced through parallel I/O ports.

The Centronics Interfaces

The four 10 and 12 pin connectors summarized in the chart below are the two Centronics Interfaces located on the Universal Parallel I/O Interface Board. Two connectors are used for each port, one for input and the other for output. This format is directly compatible with almost any printer. The output connectors contain the buffered data to be output to the device. The input connector can be used to input handshaking or status information from the device. The strobes produced are active low and are about 1 microsecond in duration.

The +5 Volt Supply provided at these connectors is drawn directly from the power supply of the H/Z89 or H8 computer. Therefore, the current capacity of this supply is limited by the loading of other peripherals in your system.

The Centronics Interfaces

Output Connector (Port #6)

1	Data Strobe (Active Low)
2	Data Bit 2
3	Data Bit 0 (LSB)
4	Data Bit 1
5	Data Bit 3
6	Data Bit 6
7	Data Bit 4
8	Data Bit 5
9	Data Bit 7 (MSB)
10	Ground

Output Connector (Port #7)

1	Data Strobe (Active Low)
2	Data Bit 2
3	Data Bit 0 (LSB)
4	Data Bit 1
5	Data Bit 3
6	Data Bit 6
7	Data Bit 4
8	Data Bit 5
9	Data Bit 7 (MSB)
10	Ground

Input Connector (Port #6)

1	Data Strobe (Active Low)
2	Data Bit 0 (LSB)
3	Data Bit 1
4	Data Bit 2
5	Data Bit 3
6	Data Bit 4
7	Data Bit 5
8	Data Bit 6
9	Data Bit 7 (MSB)
10	Ground
11	No Connection
12	+5 Volt Supply

Input Connector (Port #7)

1	Data Strobe (Active Low)
2	Data Bit 0 (LSB)
3	Data Bit 1
4	Data Bit 2
5	Data Bit 3
6	Data Bit 4
7	Data Bit 5
8	Data Bit 6
9	Data Bit 7 (MSB)
10	Ground
11	No Connection
12	+5 Volt Supply

The IGC Interface

The lower 34 pin header connector on the Universal Parallel I/O Interface Board is the IGC Interface. The buffered eight bit data bus for all six ports, six data read strobe signals, and six data write strobe signals are all provided at this one connector. The strobes produced are active low and about 1 microsecond in duration.

The IGC Interface

Ground	18	17	Data Bit Ø
Ground	19	16	Data Bit 1
Ground	2Ø	15	Data Bit 2
Ground	21	14	Data Bit 3
Ground	22	13	Data Bit 4
Ground	23	12	Data Bit 5
Ground	24	11	Data Bit 6
Ground	25	1Ø	Data Bit 7
Ground	26	9	Port #Ø Write Strobe
Ground	27	8	Port #1 Write Strobe
Ground	28	7	Port #2 Write Strobe
Ground	29	6	Port #3 Write Strobe
Ground	3Ø	5	Port #4 Write Strobe
Ground	31	4	Port #5 Write Strobe
Port #5 Read Strobe	32	3	Port #Ø Read Strobe
Port #4 Read Strobe	33	2	Port #1 Read Strobe
Port #3 Read Strobe	34	1	Port #2 Read Strobe < Keyed

The Disk Controller Interface

The upper 34 pin header connector on the Universal Parallel I/O Interface Board is the Disk System Interface. The buffered eight bit data bus for the first eight port addresses, the read and write strobes, and the local address bus are provided at this connector. The strobes produced are active low and about 1 microsecond in duration.

The Disk Controller Interface

Ground	18	17	No Connection
Ground	19	16	No Connection
Ground	20	15	No Connection
Ground	21	14	Port #0-#7 Read Strobe
Ground	22	13	Port #0-#7 Write Strobe
Ground	23	12	Ground
Ground	24	11	Local Address Bit 2
Ground	25	10	Local Address Bit 1
Ground	26	9	Local Address Bit 0
Ground	27	8	Data Bit 7
Ground	28	7	Data Bit 6
Ground	29	6	Data Bit 5
Ground	30	5	Data Bit 4
Ground	31	4	Data Bit 3
Ground	32	3	Data Bit 2
Ground	33	2	Data Bit 1
Ground	34	1	Data Bit 0 < Keyed

The CPU Control Connector

The control connector (8 pin connector) on the Universal Parallel Board provides a number of control signals which can be used for custom applications. The first three inputs (Pins 1, 2, and 3) are required by the H/Z89 version of the Universal Parallel Board to operate properly. These inputs are provided by the CPU Control Cable. Pins 1, 2, and 3 have no connection on the H8 version. Pins 4 and 5 are outputs which indicate that one of the eight port addresses of the Universal Parallel Board have been accessed, and the data flow direction for that I/O operation. Pins 6 and 7 are inputs which can be used to tristate the outputs of ports 1 and 2. These inputs are tied low through 4.7k Ohms to ground on the Universal Parallel Board.

Control Connector

1	Port I/O Enable 0 (H/Z89 Input, Active High)
2	Port I/O Enable 1 (H/Z89 Input, Active Low)
3	Processor Read (H/Z89 Input, Active Low)
4	Data Write (Output, Active Low)
5	Local Port Select (Output, Active Low)
6	Port #6 Output TriState (Input, Active High)
7	Port #7 Output TriState (Input, Active High)
8	Ground

Warranty

SigmaSoft and Systems warrants this product to be free from defective material or workmanship for a period of six months from the date of original purchase.

During this warranty period, SigmaSoft and Systems will repair, or replace at no charge, components that prove to be defective, provided the product is returned properly packed to SigmaSoft and Systems, with shipping charges prepaid.

This warranty does not apply if, in the opinion of SigmaSoft and Systems, the product has been damaged by accident, misuse, or improper installation. Furthermore, this warranty is void for hard disk drive products that have been subjected to excessive amounts of shock or vibration as specified in this manual.

This warranty is in lieu of all other representations or warranties expressed or implied. Under no circumstances shall SigmaSoft and Systems be liable for any loss or damage arising out of the use of, or inability to use, this product.

Repair Service

The SigmaSoft Disk System products are extremely reliable and with proper care should never need service. However, this support is available directly from the manufacturer, SigmaSoft and Systems, in the event that trouble does arise.

If you experience a problem, first call or write SigmaSoft for technical help. Often a problem can be solved by simply identifying an installation or configuration error. If the product is malfunctioning, the problem can usually be isolated to one specific board or cable. Be sure to mention any special modifications or non-Heath products which you are using in conjuction with your computer, such as speed-up modifications, custom interfaces, BIOS changes, etc.

Equipment returned for repair should be well packed with surrounding shock absorbing material and shipped insured to the following address.

SigmaSoft and Systems
17000 Dallas Parkway, #207
Dallas, TX 75248

The standard service fee for products out of warranty is $15. This fee must be included with the returned products as well as a detailed description of the problem and a phone number where you can be reached. There may be additional charges for replacement parts, excessive service times, or return shipping.

The following chart lists all of the parts used to assemble the SigmaSoft Disk System products. This chart is provided as an aid to those who wish to service SigmaSoft equipment themselves.

All of the following parts are available from SigmaSoft and Systems. Alternate sources are also listed. Parts which do not specify any source, are difficult to locate and should be ordered from SigmaSoft. Parts which specify SigmaSoft can only be obtained from SigmaSoft. Prices given are for SigmaSoft only and are subject to change without notice.

Guide to Replacement Parts

Description	Part Number	Sources	Price
Descrete Components			
1/4 Watt Resistor	1k Ohms	J, R, H	.Ø6
1/4 Watt Resistor	4.7k Ohms	J, R, H	.Ø6
Ceramic Capacitor	.Ø47 MFD	J, R, H	.15
Tantalum Capacitor	4.7 MFD	J, R, H	.8Ø
Tantalum Capacitor	47 MFD	J, R, H	4.ØØ
Radial Electrolytic Capacitor	1ØØØØ MFD		3.ØØ
3 Amp Silicon Rectifier	1N54ØØ	J, R, H	.4Ø
Connectors and Sockets			
Molex 1Ø Pin Card Edge	22-16-21Ø1	H, A	4.ØØ
Molex 25 Pin Card Edge	22-16-2251	H, A	8.ØØ
Molex 3 Pin Straight SIP Jumper	22-1Ø-2Ø31	H, A	.15
Molex Jump Connector	15-29-1Ø24	H, A	.52
Molex 8 Pin Straight SIP	22-27-2Ø81	A	.4Ø
Molex 1Ø Pin Straight SIP	22-27-21Ø1	A	.5Ø
Molex 12 Pin Straight SIP	22-27-2121	A	.6Ø
Molex 8 Pin Shell	22-Ø1-2Ø85	A	.46
Molex 1Ø Pin Shell	22-Ø1-21Ø5	A	.68
Molex 12 Pin Shell	22-Ø1-2125	A	.68
Molex Small Spring Pin	Ø8-5Ø-Ø114	A, H	.14
Molex Large Spring Pin	Ø8-5Ø-Ø1Ø5	A, H	.14
Molex Male Pin		A, H	.16
Molex Female Pin		A, H	.16
34 Pin Right Angle PCB Header		R, H	3.6Ø
2Ø Pin IDC Socket Connector	S2Ø	J, R, H	3.ØØ
34 Pin IDC Socket Connector	S34	J, R, H	4.18
34 Pin IDC Plug Connector	P34	J, R, H	5.ØØ
2Ø Pin IDC Edge Card Connector		J, R, H	5.ØØ
34 Pin IDC Edge Card Connector		J, R, H	8.ØØ
Low Profile IC Socket	14 Pin LP	J, R, H	.7Ø
Low Profile IC Socket	2Ø Pin LP	J, R, H	1.ØØ
Low Profile IC Socket	24 Pin LP	J, R, H	1.2Ø
Molex 2 Pin Straight Power	Ø9-65-1Ø21	A	.16

Molex 3 Pin Straight Power	09-65-1031	A	.50
Molex 2 Pin Power Shell	09-50-3021	A	.50
Molex 3 Pin Power Shell	09-50-3031	A	.50
Molex 3 Pin AC Plug Shell	432-148	H	.80
Molex 3 Pin AC Socket Shell	432-149	H	.80
AMP 4 Pin Power Plug Shell		H	1.00
AMP 4 Pin Power Socket Shell		H	1.00

Integrated Circuits

Hex Inverter	74LS04	J, A, H	.70
8 Input Nand Gate	74LS30	J, A, H	.58
Quad Or Gate	74LS32	J, A, H	.78
Dual D Flip Flop	74LS74	J, A, H	.98
Binary to Decimal Decoder	74LS154	J, A, H	2.58
TriState Octal Buffer	74LS244	J, A, H	2.98
TriState Bidirectional Buffer	74LS245	J, A, H	2.98
Octal Transparent Latch	74LS373	J, A, H	2.98
TriState Bidirectional Buffer	74LS640	J, A, H	3.00

Cables

CPU Control Cable	S	12.00
Standard Floppy Cable	S	10.00
Disk Controller Backplate Cable	S	10.00
Controller Interface Cable	S	10.00
34 Conducter Drive Cable	S	5.00
20 Conductor Drive Cable	S	5.00
AC Input Cable	S	2.00
AC Output Cable	S	2.00
Controller Power Cable	S	3.00

Hardware

Shoulder Spacer		.30
#4 Bolt 1/4"	H	.08
#4 Bolt 3/8"	H	.08
#4 Lock Washer	H	.04
#4 Nut	H	.06
#6 Bolt 3/8"	H	.08
#6 Bolt 1 1/4"	H	.80
#6 Lock Washer	H	.04
#6 Nut	H	.06
Wire Tie	H	.15
Controller Mounting Bracket	S	12.50

Miscellaneous

Split Bobbin Power Transformer	8V at 1.9 Amps		12.5Ø
+5V 3.ØA TO3 Voltage Regulator	LM323K	J, R, H	5.ØØ
Low Profile TO3 Heat Sink	672-3B	J, H	2.ØØ
16 Pin 8 Resistor DIP Pack 47	4116R-ØØ147Ø	A	3.ØØ
1Ø Pin 9 Resistor SIP Pack 1k	431ØR-1Ø1-1Ø2	A	2.ØØ
1Ø Pin 9 Resistor SIP Pack 4.7k	431ØR-1Ø1-472	A	2.ØØ
IGC Power Supply PC Board	Bare LPS	S	1Ø.ØØ
Universal Parallel I/O PC Board	Bare PIO	S	5Ø.ØØ
1Ø Megabyte 3.5 Inch Hard Disk Drive			495.ØØ
2Ø Megabyte 3.5 Inch Hard Disk Drive			685.ØØ
1Ø Megabyte 5.25 Inch Hard Disk Drive			445.ØØ
2Ø Megabyte 5.25 Inch Hard Disk Drive			495.ØØ
WD1ØØ2 Disk Controller			195.ØØ
External Drive Cabinet with 5Ø Watt Power Supply			195.ØØ

Recommended Sources of Supply

Code	Company Name and Address	Comments
S	SigmaSoft and Systems 4488 Spring Valley, #1Ø7 Dallas, TX 75234 (214) 392-1Ø25	Phone Orders, COD ($3.ØØ), Credit Cards, $3.ØØ Shipping for Small Part Orders
J	Jameco Electronics 1355 Shoreway Road Belmont, CA 94ØØ2 (415) 592-8Ø97	Good Prices and Delivery, Phone Orders, COD, Credit Cards, $2Ø.ØØ Minimum
A	Hamilton Avnet Electronics 2111 West Walnut Hill Lane Irving, TX 75Ø62 (214) 659-4111	Parts Distributor, Good Prices and Delivery, Phone Orders, COD, No Minimum
H	Heath Company Parts Department Benton Harbor, MI 49Ø22 (616) 982-3571	Good Delivery, Phone Orders, COD, Credit Cards, Must Have Heath Part Numbers
R	Radio Shack Stores	Local Stores, Poor Stock

Introduction

The following information is provided to aid experienced assembly language programers with understanding the fundamental data areas and proceedures used by the SigmaSoft disk system software support package. An understanding of this information is not required to use any of the disk system's features or capabilities. This section does however provide the necessary information to create new systems level interface software that would be compatible with the SigmaSoft products.

Another important application of this section would be to recover information that was stored on a hard disk drive using the SigmaSoft products that was lost due to damage in the special data areas on cylinder zero of the drive.

Disk Format Tables

The following chart summarizes the organization of the drive format tables on the first cylinder of the hard disk. The HDFORMAT utility builds these tables onto all available surfaces of this cylinder at the end of a format operation. These tables are vital to the operation of the SigmaSoft hard disk support software package.

Summary of Format Tables on Drive Cylinder Zero

Sector Numbers	Contents
Ø Only	Label Sector
1 Through 8	Software Boot Code (SBC)
9 Only	Partition Information Table
1Ø Only	Reserved for Future Use
11 Through 12	Bad Sector List

Detail of Label Sector Format

Addresses	Contents
Ø	Jump Instruction (C3H)
1	Address of Software Boot Code
3	Identification String (SigmaSoft)
12	Format Version Number
13	Format Revision Number
14	Default Boot Partition (Ø=Any,1=HDOS,2=CPM,3=MSDOS)
15	Default Boot Partition Name
26	Reserved for Future Use (Should be Zero)
3Ø	Total Drive Cylinder Count
32	Total Drive Head Count (Surfaces)
34	Cylinder Number to Begin Write Precompensation
36	Cylinder Number for Parking Heads
38	Drive Step Rate Code for Drive Controller
4Ø	Count of Sectors per Track
42	Count of Bytes per Sector
44	Sector Interleave Factor
46	Reserved for Future Use

Detail of Partition Information Table Format

Addresses	Contents
Ø	Partition Type Code (Ø=Free,1=HDOS,2=CPM,3=MSDOS)
1	First Cylinder Number of Partition
3	Count of Cylinders in Partition
5	Name of Partition

Detail of Bad Sector List Entry Format

Addresses	Contents
Ø	Cylinder Number of Bad Sector
2	Head Number of Bad Sector
3	Number of Bad Sector on Track

Operating System Dependent Areas

Note that the information stored in the drive format tables is generic from an operating system standpoint. However, the first 1Ø sectors of each partition are reserved for operating system dependent information. For details concerning the format of these data areas, refer to the appropriate documentation on the particular operating system involved. The format used by SigmaSoft for HDOS and CP/M boostrap areas conform to the standards established by the Heath Company.

WD1ØØ2 Disk System Bootstrap Proceedure

The SigmaROM begins the bootstrap process by reading the label and Software Boot Code (sectors Ø through 8) from the first cylinder of the hard disk and placing this information in memory at 228ØH. In the case of the WD1ØØ2 floppy disk controller, this information is actually read from the first eight sectors of the first track of the designated floppy drive. If at any time errors occur while attempting to read sectors from cylinder zero, one of the duplicate copies will be read from one of the other surfaces of the same cylinder.

Next, the SigmaROM places the I/O port address of the WD1ØØ2 disk controller in memory at 2Ø3CH and the drive select code at 2131H. The final operation of the SigmaROM boot proceedure is to transfer execution control to the Software Boot Code by loading the processor's program counter register with 228ØH.

The Software Boot Code begins by making a copy of itself in memory at 3ØØØH and transfering execution control to that address. The new SBC then reads the Partition Information Table from cylinder zero of the disk (sector 9) into memory to process the original boot command string. If a matching partition name is found in the Partition Table, the first 1Ø sectors of the first cylinder of the matching partition is read into memory at 228ØH. Execution control is then transferred to that address where the boostrap proceedure will begin for the particular operating system involved.

WD1002-05
Winchester/Floppy Disk
Controller
OEM Manual

Document No.: 79-000002

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TWX 910-595-1139

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INTRODUCTION

1. DOCUMENT SCOPE

This document provides the user with the information required to design related software drivers and interface connections for efficient use of the WD1002-05 Winchester/Floppy Disk Controller Board.

It is to the user's advantage to become familiar with the following related documents:

WD279X-02 Floppy Disk Formatter/ Controller Family	Data Sheet
WD1010-05 Winchester Disk Controller	Data Sheet
WD1010 Winchester Disk Controller	Application Note
WD1014 Error Detection/Support Logic Device	Data Sheet
WD1015 Buffer Manager Control Processor	Data Sheet
ST-506 Micro Winchester Disk Controller Seagate Technology Scotts Valley, CA	ST-506 S.M.

1.1 DESCRIPTION

The WD1002-05 Winchester/Floppy Disk Controller (WFC) is a stand-alone, general purpose board that allows a Host processor to control up to three Winchester 5.25-in. disk drives and four floppy 5.25-in. disk drives. The following is a synopsys of the WD1002-05 features:

- User-selectable 5.25" Winchester or Floppy operation
- controls up to 3 Winchester and up to 4 Floppy drives
- Single +5V Power Supply
- 8-bit universal host interface
- On-Board data separation circuitry
- On-Board write precompensation for floppy and hard disks
- On-Board sector buffer supports up to 1K-byte sectors
- Programmable sector sizes — 128, 256, 512, or 1024 bytes
- Automatic track formatting on hard and floppy disks
- Multiple sector operations on all disks
- Data rates up to 5 Mbits/sec on hard disk
- Single burst error correction up to 5 bits on hard disk data
- CRC generation/verification for data and **all** I.D. fields
- Automatic retries on all errors with simulated completion
- ECC diagnostic commands included (READLONG & WRITELONG)
- WD1002-05 internal diagnostics
- 16 different stepping rates for both hard and floppy drives

All buffers and driver/receivers needed for direct connection to the disk drives are furnished as part of the WD1002-05 circuitry. The logic for the WD1002-05's variable-length Sector Buffer, as well as logic necessary for error correction, data separation, and Host interface circuitry is also included. Winchester disk drive signals are based on the floppy disk, look-alike interface available with the Seagate Technology ST506 and other compatible drives.

I/O connections are made with standard ribbon cable connectors. The disk interface connectors have standard pinout configurations to allow direct pin-for-pin connection to the Winchester and Floppy disk drives. Power (+5 VDC) and ground for the WD1002-05 are furnished on a separate connector.

1 1.1 ON-BOARD PROCESSING AND CONTROL DEVICES

The WD1002-05 consists of a set of devices specifically designed for Host control of a Winchester and Floppy disk drives. The heart of the control logic is the Control Processor Buffer Manager (WD1015) that manages the on-board static RAM sector buffer. All bytes of data written to, and read from disk is first stored in this Sector Buffer. When the buffer is full, the data is transferred, on command, to its intended destination.

The WD1015, besides controlling data flow between Host, Sector Buffer, and disk controllers, also translates the Host Winchester command format to Floppy disk format when addressing the Floppy Disk Controller (WD2797). This permits the Host to maintain a single command format (Winchester) while in effect controlling two different disk command formats (Winchester vs. Floppy). This is possible since the SDH Register is used to select either type of drive.

The WD1015 maintains the current copies of necessary Host command data in the Task Files; a set of registers physically located in the Winchester Disk Control device (WD1010) and the Error Detection and Support logic device (WD1014).

The WD1010 is the link between the Host processor (via Sector Buffer) and the Winchester disk drives. During transfer of data from the Host to the WD1010 the WD1014 computes a 4-byte ECC which is appended to the data being transferred to the WD1010 and recorded on disk. During data transfers from the WD1010 to the Host (via the Sector Buffer), the WD1015 uses the ECC

syndrome to validate the data. Retries and corrections are attempted automatically in case of corrupted data.

The WD1015 performs error correction in conjunction with the WD1014 on data transferred to the disk. While the WD1015 controls the operation of the on-board error-correction logic, the WD1014 generates and checks the Error Correction Code (ECC) if SDH bit 7 = 1 Thus the WD1014 also provides the WD1015 its real-time control capability. Specifically, the real-time function is provided for Winchester disk operation only (real-time function is not available for Floppy disk operation).

If CRC format Winchester disks are used, CRC is selected by the WD1010 by setting SDH 7 = 0. CRC for the floppy disks is performed by the WD2797, a device that furnishes all control functions for floppy disk drives, including necessary data separation and write precompensation. SDH7 must be set to zero for floppy disk operation.

A simplified data flow and command flow block diagram is illustrated in Figure 1-1

1.1.2 COMMUNICATIONS BETWEEN HOST AND WD1002-05

Two-way communications between the Host processor and the WD1002-05 is via a parallel access port and an 8-bit, bi-directional bus. Appropriate control signals are used to transmit disk READ/WRITE data, status information, and macrocommands over the data bus.

Communications between the Host processor and the WD1002-05 uses eight data bus lines (DAL7-DAL0), a Card Select ($\overline{CS}$), a Read Enable ($\overline{RE}$), a Write Enable ($\overline{WE}$), three address lines (A2-A0), a Master Reset ($\overline{MR}$), a Data Request (DRQ), and an Interrupt Request (INTRQ). (See SECTION 2 for a complete description of control signals.)

The Master Reset strobe ($\overline{MR}$) must be used to initialize the WD1002-05 on power-up. This always initiates the internal diagnostics of the WD1002-05 and no command can be processed until the BUSY bit is cleared (approx. 1-2 seconds).

To communicate with the WD1002-05, the Host processor must first access a set of registers called the Task Files (see SECTION 5 for a description of the Task File Registers and SECTION 7 for programming information). All parameters necessary for a command to be executed are set into the Task Files. The Task Files tell the WD1002-05 what is to be done, i.e. sector size to be selected, disk drive selected and head or side desired, sector number, and any other information needed to execute the command.

After a command has been issued, the Host can verify that the command has been executed either by polling the BUSY bit in the Task File or by waiting for an Interrupt Request (See SECTION 6 for description of commands).

For all write operation commands, including format, the Host must fill the Sector Buffer with no less than the sector size chosen, otherwise the WD1002-05 will not execute the command. The Sector Buffer need only contain the required valid data to execute the command while the rest of the bytes serve as fillers (especially for a format operation). Once the Sector Buffer is

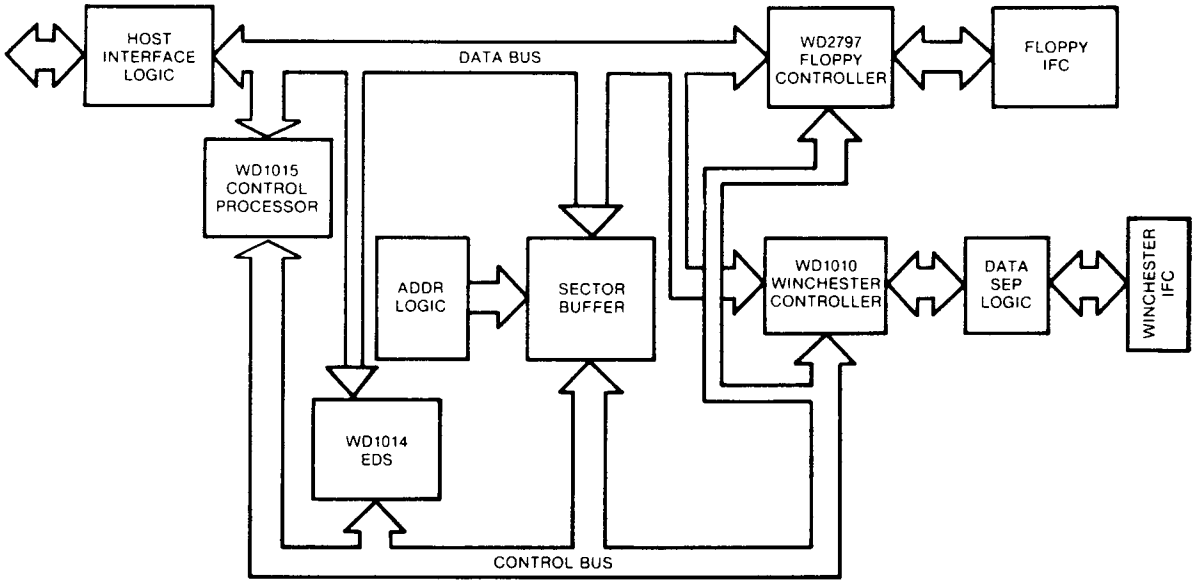


FIGURE 1-1. WD1002-05 SIMPLIFIED DATA/COMMAND FLOW BLOCK DIAGRAM

filled all communications with the Host are terminated.

Multiple transfer commands are handled one sector at a time. If the Host wants to transfer ten sectors, the WD1002-05 sequentially accepts one sector of data at a time and processes it until all sectors have been transferred. At the completion of the multiple transfer, the Interrupt Request is set, and the BUSY bit is cleared.

The Data Request (DRQ) will always be set at the start of a Write Command, indicating that the Sector Buffer is available for sequentially inputting data. If the data request is set on a Read Command, it indicates that data requested by the Host is in the Sector Buffer.

The Interrupt Request (INTRQ) is set after completion of a command. Status and error information may now be read by the Host.

1.2 SPECIFICATIONS

1.2.1 PERFORMANCE

DRIVE PARAMETERS	WINCHESTER DISKS	FLOPPY DISKS
Encoding method:	MFM	MFM
Cylinders:	Up to 1024	Up to 256
Sectors per track:	Up to 64	Up to 64
Heads:	8	2
Drive selects:	3 (ST506)	4 (SA450)
Step rate:	35 μs to 7.5 ms (500 μsec increments)	$\sim$15μs, 1ms, 2ms, 3ms, 4ms, 5ms, 6ms, 8ms, 10ms, 12ms, 14ms, 16ms, 18ms, 20ms, 25ms, 40ms.
Data transfer rate:	5.0 Mbits/s	250 Kbits/s
Write Precomp time:	12 ns	100 to 300 ns adj.
Sectoring:	Soft	Soft
	General	
CRC polynomial:	$X^{16} + X^{12} + X^5 + 1$	
ECC polynomial:	$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$	
ECC polynomial reciprocal:	$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$	
	512 byte sector	**256 byte sector**
Non-detection probability:	$\sim$2.30 E-10	$\sim$2.30 E-10
Miscorrection probability:	8.00 E-6	1.57 E-5
Correction span:	5 bits	5 bits
Single burst detection span:	20 bits	19 bits
Double burst detection span:	4 bits	3 bits
Host interface:	8-bit bi-directional bus	
Drive capability:	10 LS loads	
Drive cable length:	10 ft max	
Host cable length:	3 ft max	
Power requirements:	+5V $\pm$ 5%, 3.0 A max	
MTBF:	10,000 POH	
MTTR:	30 min.	

1.2.2 PHYSICAL

Length:	8.00 in.
Width:	5.75 in.
Height:	0.75 in.

1.2.3 ENVIRONMENTAL

Ambient temperature	0-50°C
Relative Humidity (non-condensing)	20% - 80%
Air flow	100 linear ft/min at 1/2" from component surface

SECTION 2
INTERFACE CONNECTORS

2.1 ORGANIZATION

The WD1002-05 board has seven connectors for user application:

(J6) Power connector

(J5) Host interface connector

(J7, J8) Drive control connectors

(J1, J2, J3) Winchester high speed data connectors

The drive control cables are daisy-chained to each of the three Winchester drives. The three drive data connectors carry differential signals and are radially connected.

2.2 HOST INTERFACE CONNECTOR SIGNALS

The signals of the Host interface connector (J5) are compatible with most microprocessors and many minicomputers. The connector consists of an 8-bit bi-directional bus, a 3-bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. The control signals are as follows:

DAL0-DAL7 — 8-bit, bi-directional Data Access Lines. These lines are in a high-impedance state whenever the $\overline{CS}$ line is inactive.

$\overline{CS}$ — When Card Select ($\overline{CS}$) is asserted along with $\overline{RE}$ or $\overline{WE}$, data is read or written via the DAL bus.

$\overline{WE}$ — When Write Enable ($\overline{WE}$) is asserted along with $\overline{CS}$, the Host may write data to a selected register of the WD1002-05.

$\overline{RE}$ — When Read Enable ($\overline{RE}$) is asserted along with $\overline{CS}$, the Host may read data from a selected register of the WD1002-05.

A2-A0 — Three Address lines are used to select one of the nine registers and Sector Buffer on the WD1002-05. They must remain stable during all read and write operations.

INTRQ — The Interrupt Request line is asserted whenever a command has been completed. It is de-asserted when the Status Register is read, or a new command is issued to the WD1002-05, or when $\overline{MR}$ is asserted.

DRQ — The Data Request line is asserted whenever the Sector Buffer contains data to be read by the Host, or is awaiting data to be loaded by the Host. This line is de-asserted whenever the Sector Buffer is exhausted, or when $\overline{MR}$ is asserted.

MR — The Master Reset ($\overline{MR}$) signal initializes all internal logic on the WD1002-05. Whenever $\overline{MR}$ is received by the WD1002-05, the internal diagnostics are automatically initiated. $\overline{MR}$ is also asserted at power up.

GND — All even numbered pins on this connector are to be used as signal grounds. Power grounds are available on the power connector.

2.3 40-PIN HOST INTERFACE CONNECTOR

The Host interface connector (J5) is a 40-pin vertical header. Cabling should be less than three feet long. Either flat ribbon or twisted pair cable can be used. The connector pinouts are given in Table 2-1

TABLE 2-1.
HOST INTERFACE CONNECTOR PIN DESCRIPTION

Signal Ground	Signal Pin	Signal Name
2	1	DAL0
4	3	DAL1
6	5	DAL2
8	7	DAL3
10	9	DAL4
12	11	DAL5
14	13	DAL6
16	15	DAL7
18	17	A0
20	19	A1
22	21	A2
24	23	$\overline{CS}$
26	25	$\overline{WE}$
28	27	$\overline{RE}$
30	29	Pull-up (PUP)
32	31	Not Connected
34	33	Not Connected
36	35	INTRQ
38	37	DRQ
40	39	$\overline{MR}$

2.4 WINCHESTER DRIVE CONTROL SIGNALS

The Winchester Drive Control connector (J7) is a relatively low-speed bus, daisy-chained to each of the Winchester drives in the system. To properly terminate the open collector outputs from the WD1002-05, the last drive in the daisy-chain should have a 220/330-ohm line termination resistor pack installed. All other drives should have no termination. Drive control signals are as follows:

$\overline{RWC}$ — When the Reduce Write Current ($\overline{RWC}$) signal is activated with write gate, a lower write current is used to compensate for greater bit-packing density on the inner cylinders. The $\overline{RWC}$ line is asserted when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format Commands.

$\overline{WG}$ — The Write Gate signal enables the disk write data circuitry.

$\overline{SC}$ — Seek Complete line informs the WD1002-05 that the head of the selected drive has reached the desired cylinder and has stabilized. Since Seek Complete is not checked after a Seek Command, overlapped seeks are allowed.

$\overline{TK000}$ — Track 000 indicates that the R/W heads are positioned on the outermost cylinder. This signal is sampled before each step pulse is issued.

$\overline{WF}$ — Write Fault informs the WD1002-05 that some fault has occurred on the selected drive. The WD1002-05 does not execute commands when this signal is asserted.

$\overline{HS2}$-$\overline{HS0}$ — Head Select lines ($\overline{HS2}$-$\overline{HS0}$) are used by the WD1002-05 to select a specific R/W head on the selected Winchester drive.

$\overline{IND}$ — Index is used to indicate the index point for synchronization during formatting and as a timeout mechanism for retries. This signal should pulse once every rotation of the disk.

$\overline{RDY}$ — Ready informs the WD1002-05 that the desired drive is selected and that its motor is up to speed. The WD1002-05 does not execute commands unless this line is asserted.

$\overline{STEP}$ — Step is pulsed once for every cylinder to be stepped. The direction of the step is determined by the direction line. The Step pulse period is determined by the internal Winchester stepping rate register during implied seek operations, or explicitly during Seek Commands. During auto restore, the step pulse period is determined by the seek complete time from the drive.

$\overline{DS1}$-$\overline{DS3}$ — These three Drive Select lines ($\overline{DS1}$-$\overline{DS3}$) are used to select one of three possible drives.

$\overline{DIRIN}$ — Direction In determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out, and a low defines direction as in.

2.5 5.25" WINCHESTER 34-PIN DRIVE CONTROL CONNECTOR

This drive control connector (J7) is a 34-pin vertical header on 0.10-inch centers. Cabling should be flat ribbon or twisted-pair cable less than 10 feet long. The cable pinouts are given in Table 2-2.

TABLE 2-2.
WINCHESTER DRIVE CONTROL CONNECTOR PIN DESCRIPTION

Signal Ground	Signal Pin	I/O	Signal Name
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6	O	$\overline{Write\ Gate}$
7	8	I	$\overline{Seek\ Complete}$
9	10	I	$\overline{TK000}$
11	12	I	$\overline{Write\ Fault}$
13	14	O	$\overline{Head\ Select\ 0}$
15	16		NC
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24	O	$\overline{Step}$
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32		NC
33	34	O	$\overline{Direction\ In}$

2.6 WINCHESTER DRIVE DATA CONNECTOR

Three data connectors (J1-J3) allow data to pass between the WD1002-05 and each Winchester disk drive. All lines associated with the transfer of data between a drive and the WD1002-05 system are differential in nature and may not be multiplexed. The three Winchester drive data connectors are 20-pin vertical headers on 0.10-inch centers. Cabling should be either flat ribbon or twisted-pair cable, less than 10 feet long. Cable pinouts are given in Table 2-3.

TABLE 2-3.
WINCHESTER DRIVE DATA CONNECTOR
PIN DESCRIPTION

Signal Ground	Signal Pin	I/O	Signal Name
2	1		NC
4	3		NC
6	5		NC
8	7		NC
	9		NC
	10		NC
11			GND
12			GND
	13	O	MFM Write Data
	14	O	$\overline{\text{MFM Write Data}}$
15			GND
16			GND
	17	I	MFM READ Data
	18	I	$\overline{\text{MFM READ Data}}$
19			GND
20			GND

2.7 POWER CONNECTOR

A 4-pin amp connector (J6) is provided for power and ground inputs to the board. The pinouts are given in Table 2-4.

TABLE 2-4.
POWER CONNECTOR PIN DESCRIPTION

Pin	Signal Name
1	NC
2	GROUND
3	GROUND
4	+5V regulated @ 3 amps (max)

2.8 FLOPPY DRIVE SIGNALS

The Floppy Drive Control connector (J8) is a relatively low-speed bus, daisy-chained to each of the floppy drives in the system. To properly terminate each TTL-level output signal from the WD1002-05, the last drive in the daisy chain should have line terminations as specified by the drive manufacturer. The other drives should not have any terminations. Drive control signals for the floppy disks are functionally similar to those for the hard disks, except that all data is transferred via one connector instead of the separate connectors used for the Winchester drives. Floppy drive signals are as follows:

$\overline{\text{IND}}$ — The $\overline{\text{Index}}$ line contains a reference index pulse once every disk rotation to indicate the beginning of a track.

$\overline{\text{DS3-DS0}}$ — These four Drive Select lines ($\overline{\text{DS3}}$-$\overline{\text{DS0}}$) are used to select one of four possible drives.

$\overline{\text{MO}}$ — The $\overline{\text{Motor On}}$ line is used to directly control the dc spindle motor of the floppy drive. If Motor On Mode (MOM) = 0 (user selectable jumper option) then a 40 nsec delay occurs, otherwise a one-second delay occurs after Motor On and before any reading or writing is attempted. If the floppy drive is not accessed for ~3 seconds, the motor is turned off by the WD1015. Also the drives supported must be configured so that the R/W heads are loaded when the motor is turned on. This is usually available as an option on most drives.

$\overline{\text{DIRIN}}$ — The $\overline{\text{Direction In}}$ line determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out, and a low defines the direction as in.

$\overline{\text{STEP}}$ — The $\overline{\text{Step}}$ line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the direction line. The step pulse period is determined by the internal floppy stepping rate register during implied seek operations, auto restore, or explicitly during seek and restore commands. During any restore operation, the stepping-rate period is limited to 8 msec minimum.

$\overline{\text{WD}}$ — The $\overline{\text{Write Data}}$ interface line provides data to be written on the disk. This line is enabled by write gate being active.

$\overline{\text{WG}}$ — The $\overline{\text{Write Gate}}$ output signal enables disk write data circuitry.

$\overline{\text{TR00}}$ — $\overline{\text{TR00}}$ indicates that the R/W heads are positioned on the outermost cylinder. This line is sampled before each step is issued.

$\overline{\text{WP}}$ — The $\overline{\text{Write Protect}}$ interface signal provided by the drive indicates to the WD1002-05 that a write-protected disk is installed. When write protect is active, no data can be written to the disk by the WD1002-05.

$\overline{\text{RD}}$ — The $\overline{\text{Read Data}}$ line provides the "raw data" (clock and data together) as detected by the drive logic.

$\overline{SS}$ Selects side of floppy disk to be written or read.

2.9 5.25" FLOPPY 34-PIN DRIVE CONTROL CONNECTOR

This floppy drive control connector (J8) is a 34-pin vertical header on 0.10-inch centers. Cabling should be flat ribbon or twiisted-pair cable, less than 10 feet long. The cable pinouts are given in Table 2-5.

TABLE 2-5.
FLOPPY DRIVE CONTROL CONNECTOR PIN DESCRIPTION

Signal Ground	Signal Pin	I/O	Signal Name
1	2	—	NC
3	4	—	NC
5	6	O	$\overline{\text{Drive Select 0}}$
7	8	I	$\overline{\text{Index}}$
9	10	O	$\overline{\text{Drive Select 1}}$
11	12	O	$\overline{\text{Drive Select 2}}$
13	14	O	$\overline{\text{Drive Select 3}}$
15	16	O	$\overline{\text{Motor On}}$
17	18	O	$\overline{\text{Direction In}}$
19	20	O	$\overline{\text{Step}}$
21	22	O	$\overline{\text{Write Data}}$
23	24	O	$\overline{\text{Write Gate}}$
25	26	I	$\overline{\text{Track 000}}$
27	28	I	$\overline{\text{Write Protect}}$
29	30	I	$\overline{\text{Read Data}}$
31	32	O	$\overline{\text{Side Select}}$
33	34	—	NC

SECTION 3
INTERFACE TIMING

3.1 HOST INTERFACE TIMING

3.1.1 HOST TASK FILE READ TIMING

The Task Files read by the Host are physically located in the WD1010 Winchester Disk Controller. The Error Register is located in the WD1014 EDS device, and the Status Register is implemented using TTL gates.

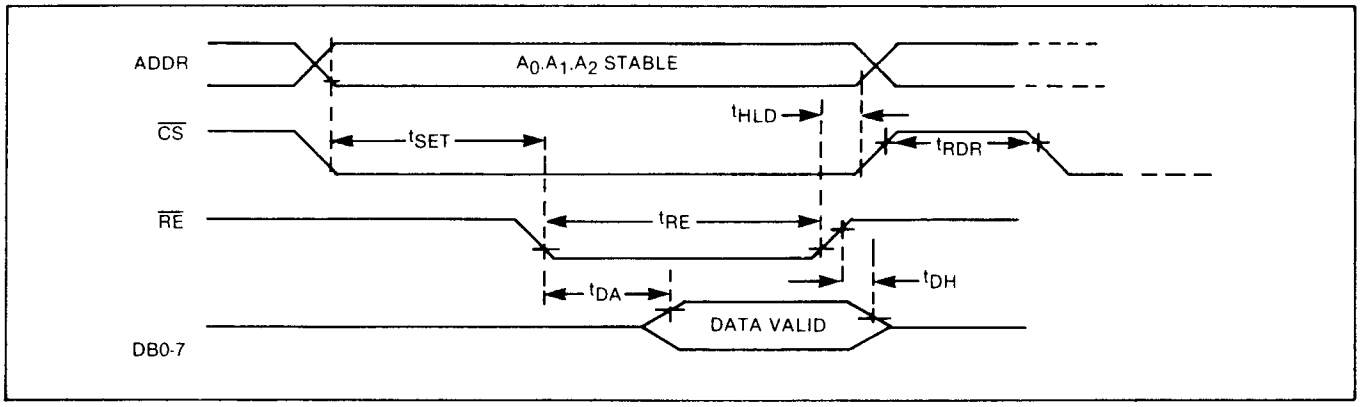


FIGURE 3-1. HOST TASK FILE READ TIMING

TABLE 3-1. HOST TASK FILE READ TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{SET}	Addr, Card select setup to $\overline{RE}$	200		nsec
t_{HLD}	Addr, Card select hold from $\overline{RE}$	0		nsec
t_{RE}	Read enable pulsewidth	0.4	10	μsec
t_{RDR}	Read Recovery time	300		nsec
t_{DA}	Data access after $\overline{RE}$ asserted		400	nsec
t_{DH}	Data hold after $\overline{RE}$ de-asserted		25	nsec

3.1.2 HOST TASK FILE WRITE TIMING

The Task Files written to by the Host are physically located in the WD1010 device except for the Command Register, which is located in the WD1014 EDS device.

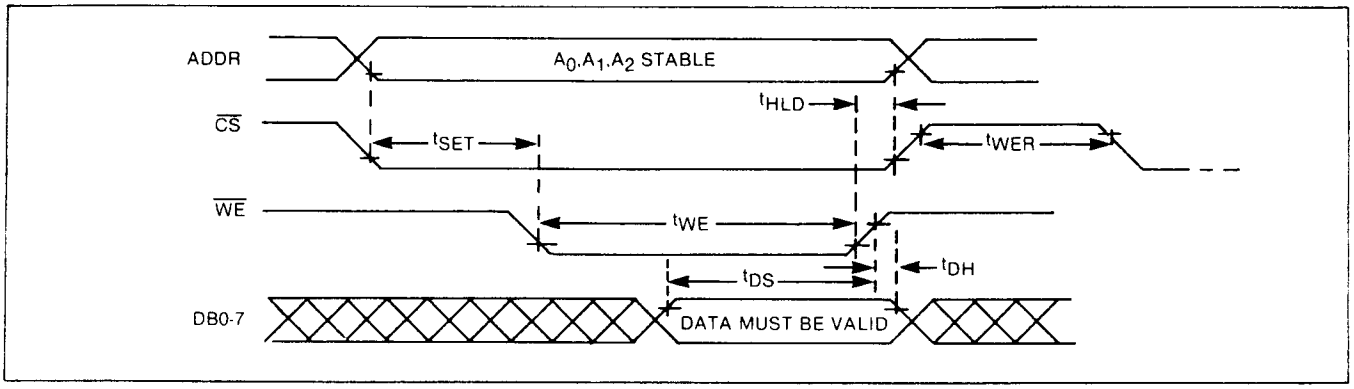


FIGURE 3-2. HOST TASK FILE WRITE TIMING

TABLE 3-2. HOST TASK FILE WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{SET}	Addr, Card select setup to $\overline{WE}$	0.1	10	µsec
t_{HLD}	Addr, Card select hold from $\overline{WE}$	30		nsec
t_{WE}	Write enable pulsewidth	0.2	10	µsec
t_{WER}	Write Recovery time	1.0		µsec
t_{DS}	Data access setup to $\overline{WE}$ asserted	0.2	10	µsec
t_{DH}	Data hold after $\overline{WE}$ de-asserted	10		nsec

3.1.3 HOST SECTOR BUFFER READ TIMING

After a Read Command, the Host reads the Sector Buffer. The DRQ line is set at the start of every sector transfer and is reset when the Sector Buffer has been emptied.

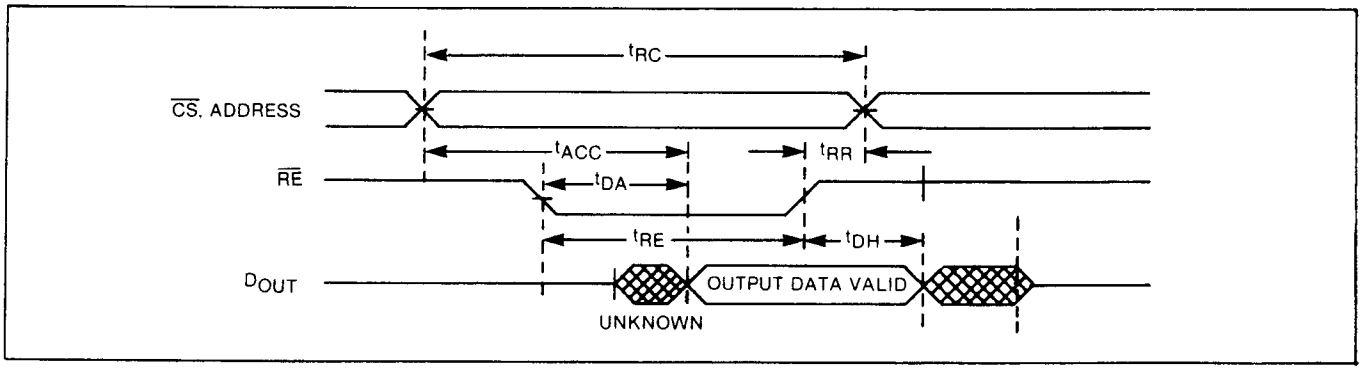


FIGURE 3-3. HOST SECTOR BUFFER READ TIMING : PROG I/O

TABLE 3-3. HOST SECTOR BUFFER READ TIMING (NORMAL MODE)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{RC}	Read Cycle time	337		nsec
t_{ACC}	Addr, Card select to Data Valid		337	nsec
t_{RE}	Read enable pulsewidth	200		nsec
t_{RR}	Read Recovery time		137	nsec
t_{DA}	Data access from $\overline{RE}$ asserted		200	nsec
t_{DH}	Data hold after $\overline{RE}$ de-asserted		25	nsec

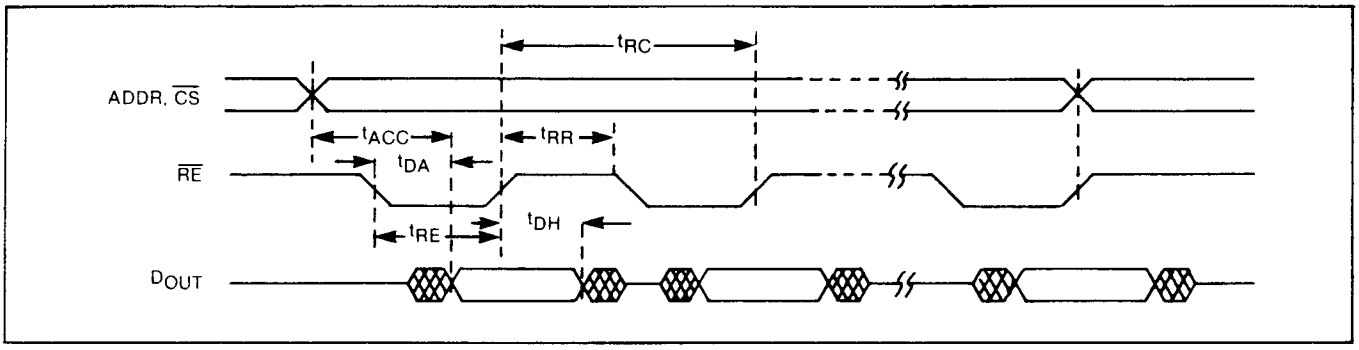


FIGURE 3-4. HOST SECTOR BUFFER READ TIMING : DMA MODE

3.1.4 HOST SECTOR BUFFER READ TIMING (LONG MODE)

In the Long Mode of Sector Buffer read timing, the Host reads four extra check bytes after the Sector Buffer has been emptied. These bytes are actually read from the WD1014 EDS device and not from the Sector Buffer. The Host is only required to generate four additional read strobes subject to the timings indicated. Multiple sector transfers are also permitted.

DMA data transfer speed should be limited in order to read the four check bytes in this special diagnostic mode.

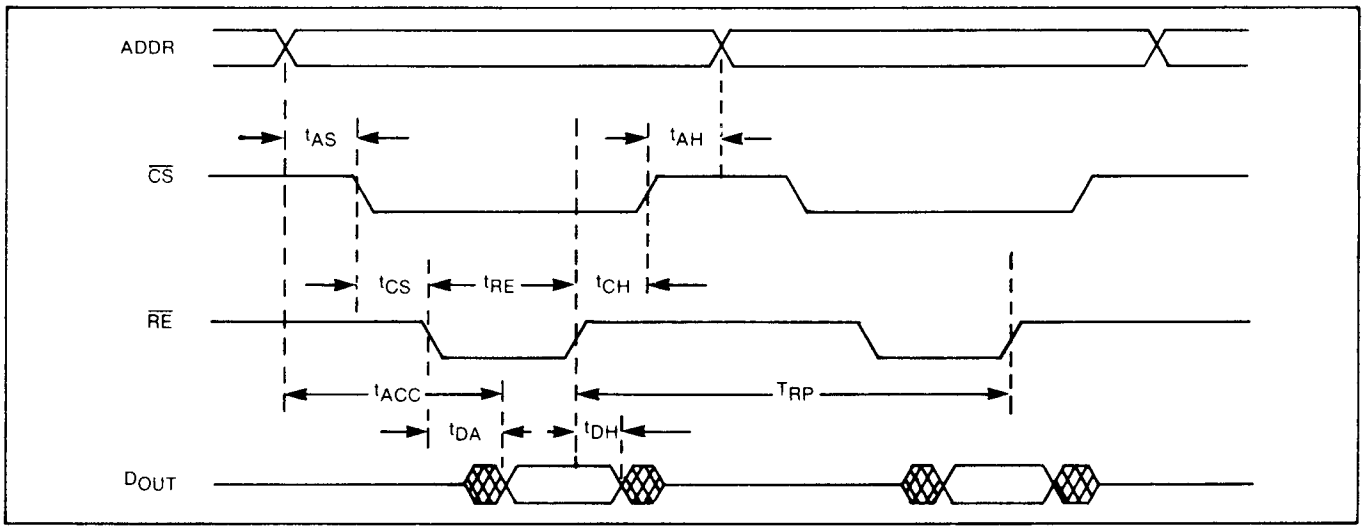


FIGURE 3-5. HOST SECTOR BUFFER READ TIMING (LONG MODE)

TABLE 3-4. HOST SECTOR BUFFER READ TIMING (LONG MODE)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{RP}	Read Cycle time	800		nsec
t_{AS}	Address setup to $\overline{CS}$	0		nsec
t_{AH}	Address hold from $\overline{CS}$	0		nsec
t_{CS}	Card select setup to $\overline{RE}$	0		nsec
t_{CH}	Card select hold to $\overline{RE}$ inactive	0		nsec
t_{ACC}	Addr, Card select to Data Valid		237	nsec
t_{RE}	Read enable pulsewidth	50		nsec
t_{DA}	Data access from $\overline{RE}$ asserted		100	nsec
t_{DH}	Data hold after $\overline{RE}$ de-asserted		25	nsec

3.1.5 HOST SECTOR BUFFER WRITE TIMING

After a Write or Format Command has been issued, the Host can write to the Sector Buffer. Both the address lines A2-A0, and the $\overline{CS}$ line can be held in their active states while writing to the sector. The DRQ signal is asserted at the start of every data transfer and is de-asserted when the Sector Buffer has been filled.

The DMA write cycle timing diagram is similar to the DMA read cycle timing shown in Figure 3-4.

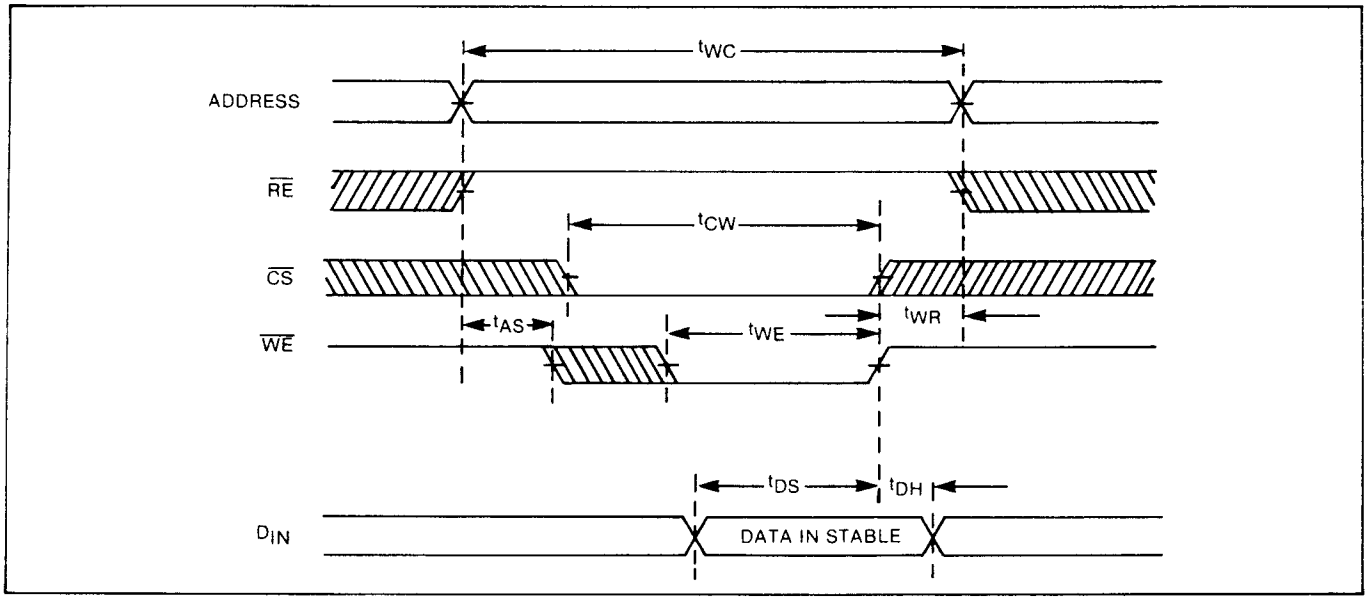


FIGURE 3-6. HOST SECTOR BUFFER WRITE TIMING (NORMAL MODE)

TABLE 3-5. HOST SECTOR BUFFER WRITE TIMING (NORMAL MODE)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{WC}	Write Cycle time	257		nsec
t_{AS}	Address setup time	0		nsec
t_{CW}	Addr, Card select to end of $\overline{WE}$	257		nsec
t_{WE}	Write enable pulsewidth	120		nsec
t_{WR}	Write Recovery time		137	nsec
t_{DS}	Data access from $\overline{WE}$ asserted	60		nsec
t_{DH}	Data hold after $\overline{WE}$ de-asserted	15		nsec

3.1.6 HOST SECTOR BUFFER WRITE TIMING (LONG MODE)

In the Long Mode of Sector Buffer write timing, four extra check bytes are written by the Host after the Sector Buffer has been filled. The bytes are actually written to the WD1014 EDS device and not to the Sector Buffer.

The Host is required to generate four additional write strobes subject to the timings indicated. Multiple sector transfers are permitted.

DMA data transfer speed should be limited in order to write the four check bytes in this special diagnostic mode.

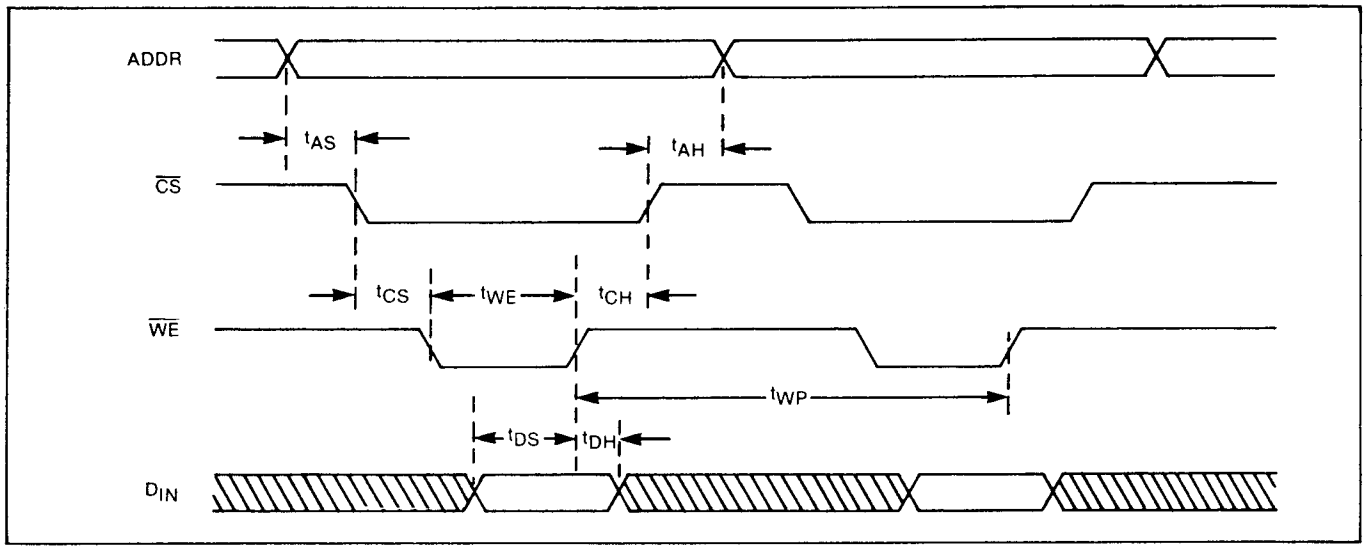


FIGURE 3-7. HOST SECTOR BUFFER WRITE TIMING (LONG MODE)

TABLE 3-6. HOST SECTOR BUFFER WRITE TIMING (LONG MODE)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{WP}	Write Cycle time	800		nsec
t_{AS}	Address setup to $\overline{CS}$	0		nsec
t_{AH}	Address hold from $\overline{CS}$	0		nsec
t_{CS}	Card select setup to $\overline{WE}$	0		nsec
t_{CH}	Card select hold to $\overline{WE}$ de-asserted	0		nsec
t_{WE}	Write enable pulsewidth	50		nsec
t_{DS}	Data setup to $\overline{WE}$ asserted	60		nsec
t_{DH}	Data hold after $\overline{WE}$ de-asserted	15		nsec

3.2 MISCELLANEOUS TIMING

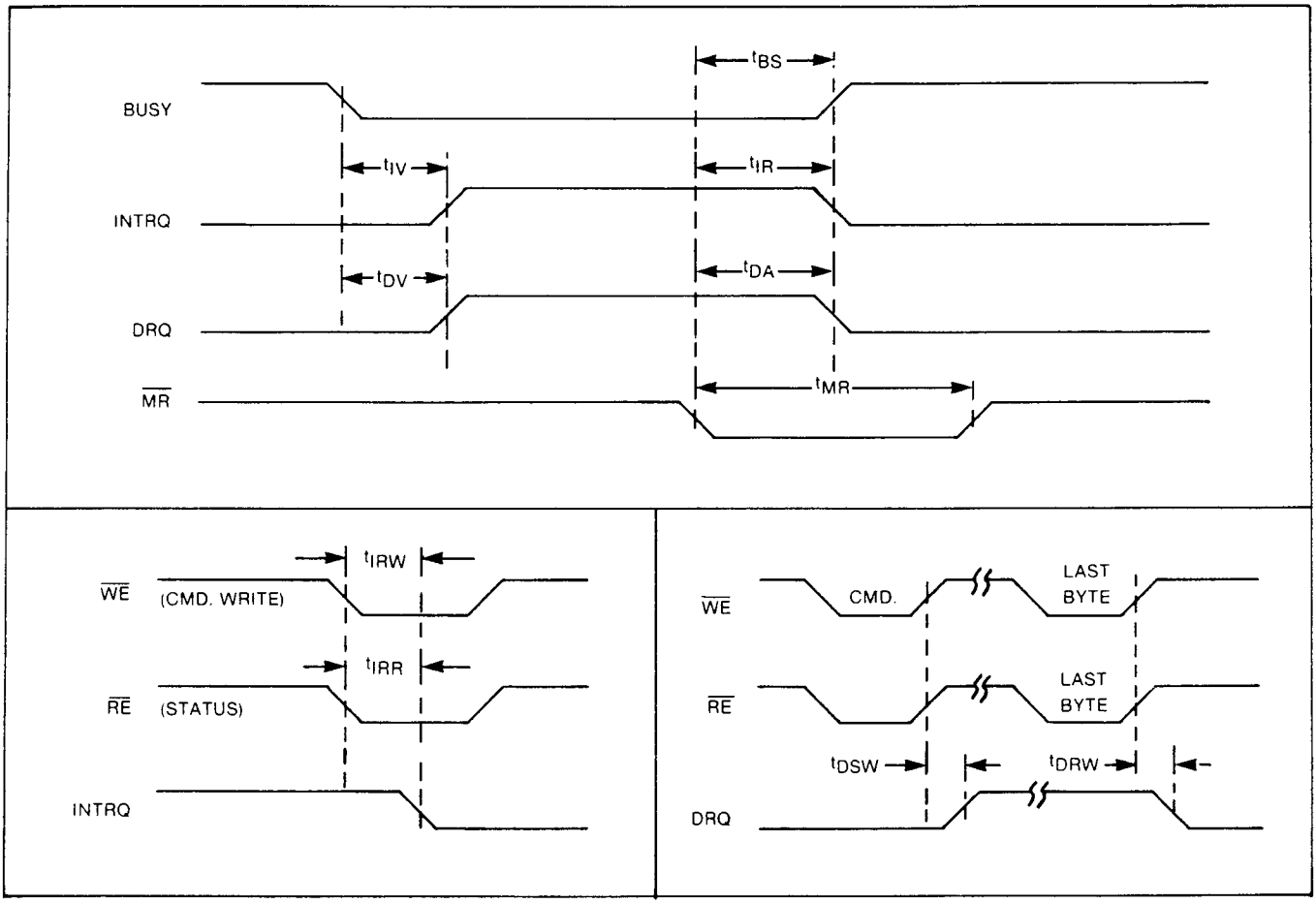


FIGURE 3-8. MISCELLANEOUS TIMING

TABLE 3-7. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS
t_{IV}	INTRQ valid from BUSY inactive		60	nsec
t_{DV}	DRQ valid from BUSY inactive		60	nsec
t_{MR}	Master Reset pulsewidth	50		msec
t_{BS}	$\overline{MR}$ to BUSY set		200	nsec
t_{IR}	$\overline{MR}$ to Interrupt reset		200	nsec
t_{DR}	$\overline{MR}$ to Data request reset		200	nsec
t_{IRW}	$\overline{WR}$ (cmd.) to Interrupt reset		200	nsec
t_{IRR}	$\overline{RE}$ (status) to Interrupt reset		200	nsec
t_{DSW}	Write command to DRQ set		200	nsec
t_{DRW}	$\overline{WE}$/$\overline{RE}$ to DRQ reset		300	nsec

SECTION 4
HOST INTERFACING

4.1 GENERAL

The WD1002-05 easily interfaces with most microcomputers and many minicomputers. Interfacing is accomplished with the Host interface connector (J5).

The interface is very similar to that used for other Western Digital LSI peripheral devices, and the signal pinouts are compatible with the Western Digital WD1000 and WD1001 series of Winchester Disk Controller boards.

The $\overline{\text{WAIT}}$ line is not used in the WD1002-05. The $\overline{\text{WAIT}}$ signal, however, is still provided for compatibility with WD1000 and WD1001 controllers.

4.2 HOST INTERFACING EXAMPLE

Figure 4-1 shows the minimum hardware required to interface the WD1002-05 board to a small 8085 microcomputer system. In the illustration, buffers are not used, nor is the I/O completely decoded. The user will most likely want to completely decode the I/O to minimize the amount of I/O or memory space required in the Host for WD1002-05 interfacing. If the interface cable length is kept to a few inches, it is often possible to directly interface the WD1002-05 to the buffered bus of a Host microcomputer.

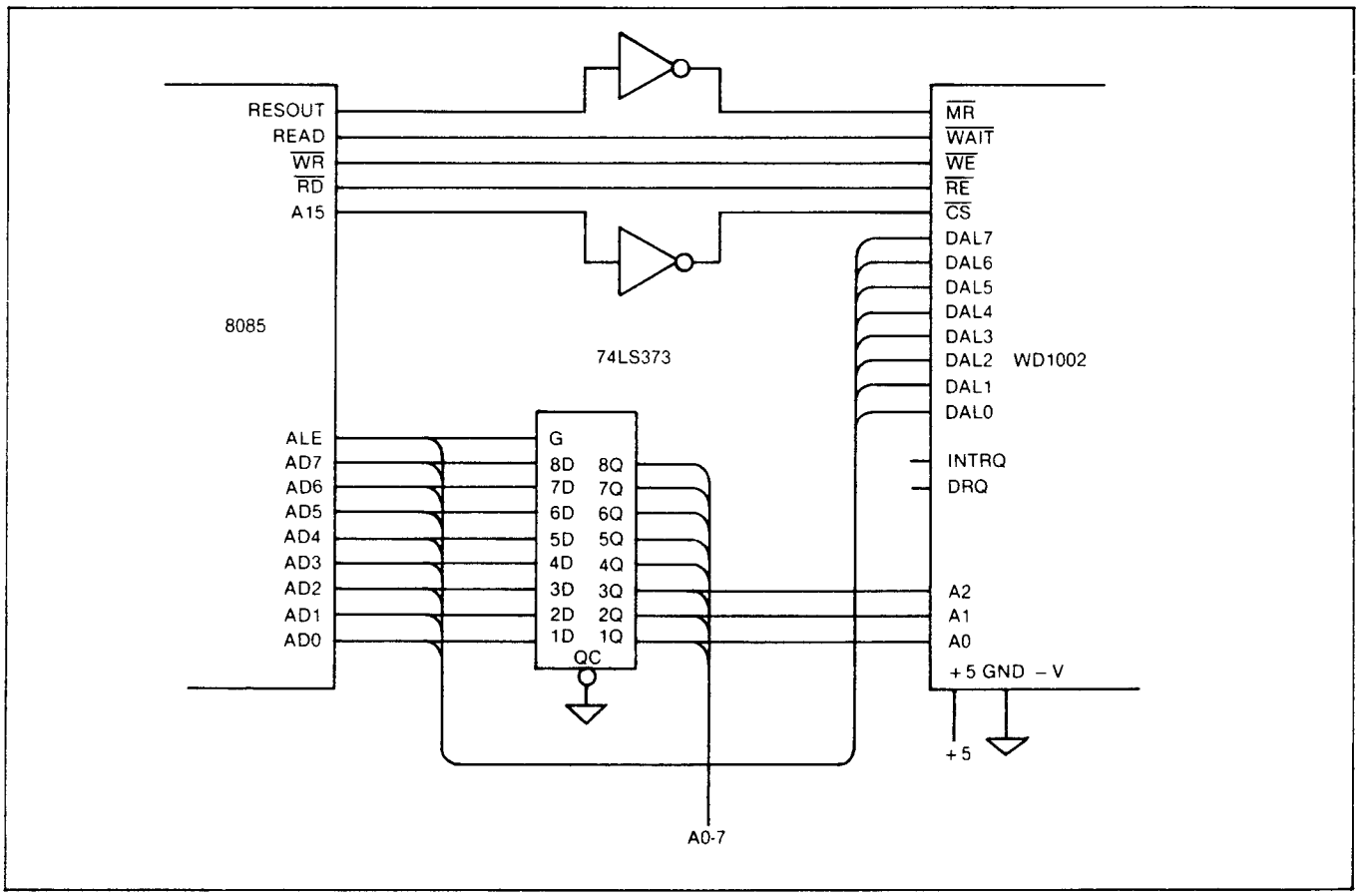


FIGURE 4-1. HOST INTERFACING EXAMPLE

SECTION 5
TASK FILE

5.1 TASK FILE BASICS

The WD1002-05 performs all disk functions through a set of registers called the Task Files. The Task Files are loaded with parameters such as sector number, cylinder number, etc., prior to issuing a command. Individual registers are selected via A0-A2 for both types of drives. The registers shown in Table 5-1 are available.

TABLE 5-1. TASK FILE REGISTER ARRAY

$\overline{CS}$	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Sector Buffer	Sector Buffer
0	0	0	1	Error Register	Write Precomp*
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High**	Cylinder High**
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

*Not used on floppies
**LSB of cylinder high, if set to 1, permits a 48 t.p.i. floppy disk to be read on a 96 t.p.i. floppy disk system.

5.2 SECTOR BUFFER

When the DRQ (Data Request) line is asserted, the Sector Buffer contains data to be read during a Type II command, or is awaiting data to be written during a Type III command. If the WD1002-05 is interfaced using programmed I/O, data transfers to this register can be implemented using programmed block moves. This register may not be read from or written to except in the context of a valid command.

5.3 WD1002-05 ERROR REGISTER

This Register contains specific fault information pertaining to the last command executed. This register is only valid if the Error Bit in the Status Register is set. The Error Register is read only. Table 5-2 shows the Error Register bits.

TABLE 5-2. ERROR REGISTER BITS

Bit	Normal Operation Status Req. Bit 0 = 1	Diagnostic Operation Status Req. Bit 0 = 0
7	Bad Block Detect	
6	Uncorrectable Error	
5	CRC Error ID Field	WD1015 Error
4	ID Not Found	WD1014 Error
3	—	Sector Buffer Error
2	Aborted Command	WD1010 Error
1	TK000 Error	WD2797 Error
0	DAM not found	Pass — WD1002 is Functional

DAM NOT FOUND — Is set during a Read Sector Command if, after successfully identifying the ID field, the Data Address Mark was not detected within 16 bytes of ID field.

TK000 ERROR — Is set during a Restore Command if the track 000 line was not asserted by the drive after all stepping pulses have been issued. The Winchesters are issued a maximum of 1023 stepping pulses and the floppies, a maximum of 256 stepping pulses.

ABORTED COMMAND — Indicates that a valid command has been received that cannot be executed based on status information from the drive, i.e. drive not ready, seek complete not asserted, or write fault. Interrogation of the Status Register by the Host may be performed to determine the cause of this failure.

ID NOT FOUND — When set, this bit indicates that an ID field containing a specified cylinder, head, sector number, or sector size was not found after all the retries have been executed.

UNCORRECTABLE ERROR	Indicates that an ECC or CRC error was encountered in a data field during a Read Sector Command and the error was uncorrectable.
BAD BLOCK DETECT	Indicates that a Bad Block Mark has been detected in the specified ID field. If the command issued was a Write Sector Command, Write Gate may be pulsed but the sector will not be written. If generated from a Read Sector Command, the data field is not read. Note that bad block may not be detected if there is a flaw in the ID field.

5.4 DIAGNOSTIC ERRORS

On power-up, or when specifically commanded to, the WD1002-05 runs a series of internal diagnostic tests. When an error is encountered, the diagnostic routine is terminated. A binary error code is set in the Error Register without the error bit of the Status Register being set. The diagnostic routines are exercised in the following order: (Refer to table 5-2)

Error Code	Major Functional Failure
5	WD1015 error
4	WD1014 or bus error
3	sector buffer error
2	WD1010 error
1	WD2797 error
0	Pass — WD1002-05 is functional

5.5 WRITE PRECOMP

The Write Precompensation Register holds the cylinder number where the RWC line will be asserted and write precompensation logic is to be turned on. This write-only register is loaded with the cylinder number divided-by-4 to achieve a range of 1024 cylinders. For example, if write precompensation is desired for cylinder 128 (80 Hex) and higher, this register must be loaded with 32 (20 Hex). The write precompensation delay is fixed at 12 nanoseconds from nominal.

This register is not used for floppy disk drives. Floppy disk write precompensation is contained in WD2797 and set as described in the "Summary of Adjustment Procedure" in SECTION 9 (MAINTENANCE) of this manual.

5.6 SECTOR COUNT

The Sector Count Register is used in Read Sector, Write Sector, and Format Commands to implement multiple sector handling with one command. The value of zero implies a transfer of 256 sectors (any size). For Read and Write multiple sector commands, the sector count is decremented, and the sector number is incremented after each sector transfer to or from the buffer. During a Format Command, this register is loaded with the number of sectors to be formatted and decremented as each sector is formatted until it reaches zero. During format, sector numbers are specified using interleave tables loaded in the sector buffer.

5.7 SECTOR NUMBER

This register is loaded with the desired sector number prior to a Read or Write Command. The Sector Number Register may be read or written by the Host.

5.8 CYLINDER NUMBER

These two registers form the cylinder number where the head is to be positioned on a Seek, Read, or Write Command. The two least significant bits of the Cylinder High Register form the most significant bits of the cylinder number as illustrated below:

	Cylinder High								Cylinder Low							
Register bits:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Cylinder bits:							9	8	7	6	5	4	3	2	1	0

When bit 0 of the Cylinder High Register (bit 8 of cylinder register) is set to a 1 during floppy operation, 48 tpi disks can be used in 96 tpi disk drives for all commands. When this bit is set to 0, only 96 tpi disks can be used.

5.9 SDH REGISTER

This register contains the ECC/CRC sector size, drive select, and head select bits. The SDH Register is a read/write register organized as shown in Tables 5-3 through 5-7.

TABLE 5-3. SDH REGISTER

Bit	7	6 5	4 3	2 1 0
Function	CRC/ ECC	Sec Size	Drive Select	Head/ Drive Select

TABLE 5-4. SDH BITS 6 & 5

Bit 6	Bit 5	Sector Size
0	0	256 Bytes
0	1	512 Bytes
1	0	1024 Bytes
1	1	128 Bytes

TABLE 5-5. SDH BITS 4 & 3

Bit 4	Bit 3	Drive Selected (decoded & latched)
0	0	Drive Sel 1
0	1	Drive Sel 2
1	0	Drive Sel 3
1	1	Floppy Dr Sel

TABLE 5-6. SDH BITS 2, 1 & 0 HARD DISK

Bit 2	Bit 1	Bit 0	Head Selected Hard Disk
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

The SDH Register is used to select either the Winchester or the floppy disk drives as implied by bits 3 and 4 shown in Table 5-5. If either bit is set to zero, then one of the hard disks is selected, and Table 5-6 is used to select one of eight heads.

When bits 3 and 4 are both set to 1, then a floppy disk will be selected. Table 5-7 is used to select one of four drives with side select 0 or 1 as shown.

Whenever different drives are to be accessed, the SDH Register must be updated by the Host prior to a command being issued.

TABLE 5-7. SDH BITS 2, 1 & 0 FLOPPY DISK

Bit 2	Bit 1	Bit 0	Floppy Drive & Head Select
0	0	0	FD1 — HS0
0	0	1	FD1 — HS1
0	1	0	FD2 — HS0
0	1	1	FD2 — HS1
1	0	0	FD3 — HS0
1	0	1	FD3 — HS1
1	1	0	FD4 — HS0
1	1	1	FD4 — HS1

5.10 STATUS REGISTER

After execution of a command, the Status Register is loaded with status information pertaining to the command executed. The Host must read this register to ascertain successful execution of the command. The Status Register is a read-only register; it cannot be written to by the Host. If the BUSY bit is set, no other bits in this register are valid. Accessing this register will cause the INTRQ line to be de-asserted.

Status register bits are shown in Table 5-8.

TABLE 5-8. STATUS REGISTER BITS

Bit	Status Register
7	Busy
6	Drive Ready
5	Write Fault
4	Seek Complete
3	Data Request
2	Corrected Data
1	Not used
0	Error

ERROR — When set, indicates that one or more bits are set in the Error Register. It provides an efficient means of checking for an error condition by the Host. This bit is reset on receipt of a new command.

CORRECTED DATA — This bit indicates that an error correction has been successfully completed on the data field just read from the Winchester disk. For multiple mode operations, this bit indicates one or more data fields have been successfully corrected. If an uncorrectable error occurs, the command is terminated with the appro-

	priate bit being set in the Error Register.
DATA REQUEST	Functions the same as the DRQ signal. When asserted, it indicates that the Sector Buffer is ready to accept data or contains data to be read by the Host. The Data Request bit is de-asserted when the Sector Buffer has been fully read or written. Normally, the Host need not consult this bit to determine if a byte should be transferred.
SEEK COMPLETE	Indicates the condition of the Seek Complete line on the selected Winchester drive. For Floppy drives, this signal is asserted when the SDH Register is reloaded.
WRITE FAULT/ WRITE PROTECT	Indicates the condition of the Write Fault signal on a selected Winchester drive. The WD1002-05 does not execute any command if this bit is set. If a write-protected disk is sensed in a selected floppy drive during a write operation, the Write Fault bit is set. The command is then aborted and no writing takes place.
READY	Indicates the condition of ready signals on drive. WD1002-05 does not execute any commands unless the ready bit is asserted. Normally this line is asserted for Floppy drives when the SDH Register selects any floppy drive. A user available jumper option can be implemented if the READY line is available from the floppy drive.
BUSY	After issuing a command, or initializing WD1002-05 internal diagnostics, this bit is set indicating that the WD1002-05 is busy executing a command. No other bits or registers are valid when this bit is set.

5.11 COMMAND REGISTER

All commands are loaded into this register after the Task Files have been set. Writing to this register causes the INTRQ Line to be reset. The Command Register is a write-only register. Refer to SECTION 6 (COMMANDS), subsection 6.1 for further details.

SECTION 6
COMMANDS

6.1 GENERAL

The WD1002-05 executes six, easy-to-use, macro commands. Most commands feature automatic "implied" seek, which means the Host system need not tell the WD1002-05 where the R/W heads of each drive are nor when to move them. The controller automatically performs all retries on errors encountered, including data ECC errors. If the R/W head mis-positions, the WD1002-05 automatically performs a restore and a re-seek. If the error is completely unrecoverable, the WD1002-05 simulates a normal completion to simplify the Host's software.

The commands executed by the WD1002-05 are mapped to the commands supported by the two disk controllers. The format of the WD1002-05 commands is the same as that of the WD1010 commands. The onboard WD1015 buffer manager translates this format for the WD2797, transparent to the user. Error correction and the Long Modes are only supported for the Winchester Disk Controller, therefore the Host must set SDH bit 7 = 0 and L = 0 for all the commands when a floppy disk is selected.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. The Host must observe the following simple protocol:

- The Task File must be loaded prior to issuing a command. Only parameters that change from the previous command need be entered.
- For any write/format operations, the Sector Buffer must be filled with the appropriate data before the command can be executed by the WD1002-05.

No command will execute if the Seek Complete or Ready lines are false, or the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1002-05 receives a command that is not defined in Table 6-1, undefined results will occur.

6.2 WD1002-05 COMMAND SUMMARY

Commands have been divided into three types as summarized in Table 6-1

TABLE 6-1 COMMAND TYPES

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Test	1	0	0	1	0	0	0	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	I	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

L = Long bit 0 = normal mode; 1 = Long mode
M = Multiple sect 0 = Single sector; 1 = Multiple sector
I = Read interrupt: 0 = Programmed I/O Mode; 1 = DMA Mode

6.2.1 STEPPING RATES

TABLE 6-2. r_3-r_0 — STEPPING RATE

r_3-r_0	Winchester Disk Drives	Floppy Disk Drives
0000	~35 μsec	~15 μsec
0001	0.5 msec	1.0 msec
0010	1.0 msec	2.0 msec
0011	1.5 msec	3.0 msec
0100	2.0 msec	4.0 msec
0101	2.5 msec	5.0 msec
0110	3.0 msec	6.0 msec
0111	3.5 msec	8.0 msec
1000	4.0 msec	10 msec
1001	4.5 msec	12 msec
1010	5.0 msec	14 msec
1011	5.5 msec	16 msec
1100	6.0 msec	18 msec
1101	6.5 msec	20 msec
1110	7.0 msec	25 msec
1111	7.5 msec	40 msec

6.3 TYPE I COMMANDS

Type I commands do not effect transfer of data between the Host and the WD1002-05 but merely position the R/W heads of the selected drive or run diagnostics. The Restore and Seek Commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate for the drives.

6.3.1 TEST COMMAND

Bit code 1 0 0 1 0 0 0 0

The Test Command is used to run internal diagnostics for checking WD1002-05 board function. It is mainly employed to isolate faults in the board logic. This command is always executed on a $\overline{MR}$ strobe. Any faults are reported as error codes. (See Section 5.4 for a description of the error codes.)

6.3.2 RESTORE

Bit code 0 0 0 1 R3 R2 R1 R0

The Restore Command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TK000 signal is asserted. Upon receipt of the Restore Command, the BUSY bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. For Winchester operation, the actual stepping rate is determined by the Seek Complete period. For Floppy operation, a minimum stepping pulse of 8 msec. is used. However, the stepping rate field specified by the Host is saved internally for use in all future implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error Bit in the Status Register is set, an Interrupt is generated, and the BUSY bit is cleared.

Regardless of errors encountered, the internal head position register for the selected drive is cleared. The TK000 signal is sampled. If TK000 is asserted, an Interrupt is generated and the BUSY bit is reset. If TK000 is de-asserted, stepping pulses at a rate determined by the stepping rate field are issued until the TK000 line is asserted. When TK000 is asserted, the Busy bit is de-asserted and Interrupt is issued. If the TK000 signal is not asserted within 1024 stepping pulses, the TK000 Error Bit in the Error Register and the Error Bit in the Status Register are set, the BUSY bit is reset, and an interrupt is issued.

6.3.3 SEEK

Bit code 0 1 1 1 R3 R2 R1 R0

The Seek Command positions the R/W head at a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Note that the Seek Complete signal is not sampled after the Seek Command so that multiple seek operations may be started using drives with buffered seek capability.

6.4 TYPE II COMMANDS

Type II commands characteristically transfer blocks of data from the WD1002-05 buffer to the Host. This type of command has an implicit stepping rate as set by the last Restore or Seek Command.

6.4.1 READ SECTOR

Bit code 0 0 1 0 I M 0 0

With the Winchester disk selected for a read operation, and the SDH bit 7 = 1, the WD1014 computes a new set of ECC bytes as the sector is being read. After the Sector Buffer is filled, the new ECC bytes generated by the WD1014 are compared to the ones from the disk to create the syndrome. If the syndrome is not zero, an error exists. The WD1015 instructs the WD1002-05 to read the same sector again up to a maximum of eight times. If the WD1014 generates the same syndrome two consecutive times, the WD1015 attempts to correct the data. If two consecutive like syndromes have not occurred within the eight read operations or the WD1015 was not able to correct the data, an Uncorrectable Error Bit in the Error Register and the Error Bit in the Status Register, are set. Multiple sector Read Commands are modified to single sector commands and are issued a multiple number of times. The Status and Error Registers are updated for every block of data transferred.

With the Winchester disk selected for a read, and the SDH Bit 7 = 0, CRC bytes are generated by the WD1010 and compared with the ones read from the disk. If they are not the same, an error has occurred and the WD1010 instructs the WD1002-05 to attempt to read the sector again. A maximum of ten tries are made before setting the Uncorrectable Error in the Error Register and the Error in the Status Register.

During a Floppy read sector operation only CRC is used with the data fields. If a CRC error occurs in the data field, the WD1015 buffer manager attempts a maximum of 8 retries and reports the error only if it persists. Regardless of the drive accessed (Winchester or Floppy), CRC is used on all ID fields.

6.4.1.1 READLONG Command

Bit code . 0 0 1 0 I M 1 0

This command is similar to the Read Sector Command except that the ECC operation producing the syndrome is inhibited in the WD1002-05. Instead, the WD1002-05 copies the four recorded check bytes from the disk and passes them unaltered to the Host. This command is useful in debugging and verifying the ECC hardware and software. To do this, first write normally and then issue the READLONG command. The data, or the check bytes may now be altered by the Host and written to the disk using the WRITELONG command. If a Read Command is now issued, the WD1002-05 corrects it as long as the error induced is within the correction capability of the ECC polynomial. This mode is not supported for floppy disk.

6.4.1.2 DMA Read

I = DMA Read Mode

0 = Programmed I/O mode 1 = DMA Mode

The DMA bit is used to position INTRQ in relation to DRQs during the Read Sector Command. If the DMA bit is reset (I = 0), the Interrupt will occur along with the DRQ. This allows the programmed I/O Host to intervene and transfer the data from the Sector Buffer. For programmed I/O, multiple transfer is not permitted (M = 0). If the DMA bit is set (I = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data. This mode is always used with multiple sector transfers.

6.4.1.3 Normal Completion

A normal completion occurs when the WD1002-05 encounters no errors. The BUSY bit is reset. The status of the DMA bit in the command byte is examined. If this bit is reset (I = 0; programmed I/O mode), an interrupt is issued at this time. DRQ is set until all bytes of data have been read from the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.) After all the data has been moved from the buffer, the DMA bit in the command byte is consulted again. If this bit is set (I = 1, DMA mode) then an interrupt will be issued.

6.5 TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the Host to the WD1002-05 buffer. These commands have implicit stepping rates as set by the last Restore or Seek Command.

The command is not executed by the WD1002-05 controller unless the buffer has been completely filled by the Host.

6.5.1 WRITE SECTOR

Bit code 0 0 1 1 0 M 0 0

The Write Sector Command is used to write a sector of data from the Host computer to the disk. Upon receipt of the Write Command, the controller sets DRQ until the entire sector length of data has been written into the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

6.5.1.1 WRITELONG Command

Bit code 0 0 1 1 0 M 1 0

The WRITELONG Command functions similarly to the Write Sector Command except that the ECC operation that computes the ECC word is inhibited in the WD1002-05. Instead, the WD1002-05 accepts a 4-byte appendage from the Host and passes it unaltered to be written on the disk at the end of the data as check bytes. This mode is not supported for the floppy disks.

6.5.2 FORMAT TRACK

Bit code 0 1 0 1 0 0 0 0

The Format Command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format Command, the controller sets the DRQ for the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

When the buffer has been completely filled, the specified number of sectors are written and the DRQ is reset. The data field is written with 00 for the hard disks and E5 (hex) for the floppies. ECC or CRC bytes are automatically computed and written. (Figure 6-1)

Once the index is found, a number of ID and data fields are written to the disk. As each sector is written, the Sector Count Register is decremented and consequently must be updated before each format operation.

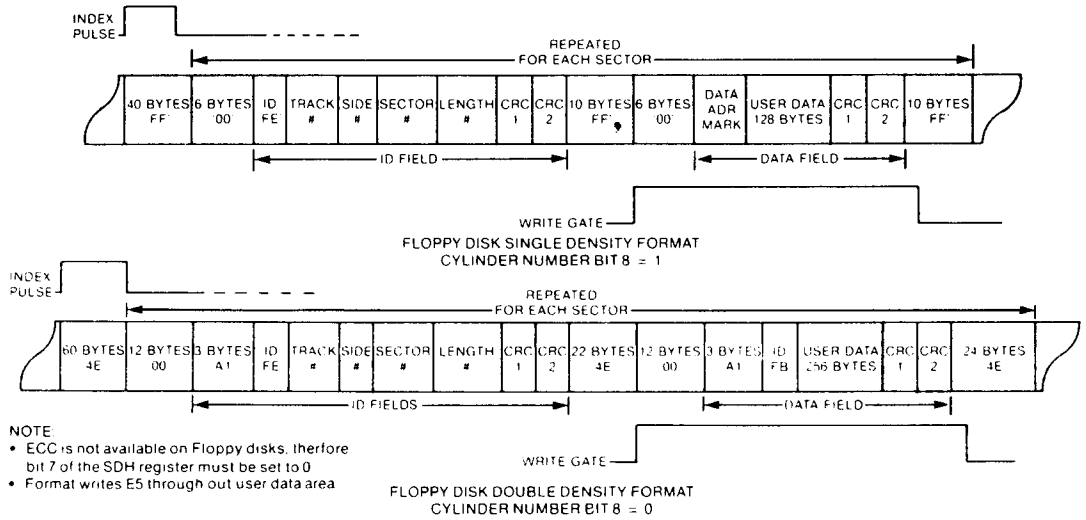


FIGURE 6-1. FLOPPY FORMAT

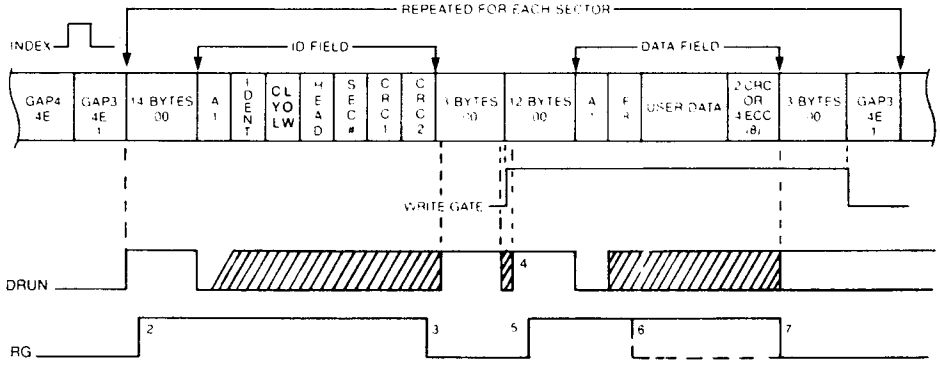


FIGURE 6-2. FORMAT

ID FIELD

A1 = A1 hex with
0A hex clock

IDENT = Bits 1, 0 = Cylinder High
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders

HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark

Sec # = Logical Sector Number

DATA FIELD

A1 = A1 hex with 0A hex clock

F8 = Data Address Mark; Normal Clock

USER = Data Field 128 to 1024 Bytes

NOTES:

1 GAP 1 and 3 length determined by Sector Number Register contents during formatting. For a Sector Length of 128 or 256 bytes the gap equals 15 bytes. Sector Length of 512 is 30 bytes. Sector Length of 1024 is 60 bytes.

2. RG asserted 2 bytes after the start of DRUN.

3. RG de-asserted:
   - If DRUN does not last until A1
   - When any part of ID does not match the one expected.
   - After CRC if correct ID has been read.

4. Write splice recorded on disk by WG being asserted.

5. RG is suppressed until after write splice.

6. Not a proper A1 or F8, set DAM error.

7. Sector size as stated in ID field, plus 2 for CRC or 4 for ECC.

8. If ECC mode, then 4 bytes of ECC plus 3 bytes pad are written.

SECTION 7
PROGRAMMING

7.1 GENERAL

Users will find programming the WD1002-05 relatively simple as a substantial amount of intelligence formerly required by Host computers has been incorporated into the WD1002-05 board.

The WD1002-05 performs all needed retries, even on head positioning errors. If there is an error in the data field, the WD1002-05 attempts to correct it.

Most commands feature automatic "implied" seek, which means that Seek Commands need not be issued to perform basic read/write functions. The WD1002-05 keeps track of the head position up to eight read/write head assemblies, eliminating the need for the Host system to maintain track tables.

All transfers to and from disk are through an on-board Sector Buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1002-05 simulates a normal completion so that special error recovery software is not needed.

This section assumes that the user has read Section 5 (Task File) and Section 6 (Commands).

7.2 SETTING UP TASK FILES

Before any of the six macrocommands can be executed, a set of parameter registers called the Task Files must be set up. For most commands, this informs the WD1002-05 of the exact location on the disk where the data involved in the transfer is located or is to be placed. For a normal read or write sector operation, the sector number, the size/drive/head, the cylinder number, and the command registers (usually in that order) will be written.

Note that although most of these registers are readable as well as writable, they normally are not read from. Read capability for them is provided, however, so that error-reporting routines can determine physically where an error occurred without recalculating the sector, head, and cylinder parameters.

Since all the Task File parameters can be recalled by the WD1002-05, it is recommended that Task File parameters be stored in the WD1002-05 as they are calculated. This saves the programmer a few instructions and microseconds by not maintaining two copies of the same information.

7.2.1 CYLINDERS AND TRACKS

Since most hard-disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder. Table 7-1 presents a cylinder-by-cylinder sequential file read on a four head, two-platter disk drive.

TABLE 7-1.
FILE READ ON 4-HEAD, 2-PLATTER DISK DRIVE

Physical Cylinder	Logical Head Number	Physical Head Side	Physical Platter
25	3	Top	B
26	0	Bottom	A
26	1	Top	A
26	2	Bottom	B
26	3	Top	B
27	0	Bottom	A

7.3 TYPE I COMMAND PROGRAMMING

Test, Restore and Seek are Type I commands that position the R/W heads of the selected drive and set the implied stepping-rate register. No data is transferred to or from the Sector Buffer. To execute a Type I command, the system software must perform the following functions in the order shown:

1. Set up Task File and issue command with stepping rate (WD1002-05 will attempt to execute Type I command)
2. Wait for Interrupt or for BUSY bit in Status Register to be reset
3. Check Error Bit in Status Register for proper completion

7.3.1 USE OF BUSY BIT

Smaller, single-user systems can sense the completion of a command by polling the BUSY bit of the Status Register. This bit (bit 7) is set whenever the controller starts a disk operation or internal diagnostics, and is reset whenever the controller is ready to communicate with the Host computer.

On the WD1002-05, the BUSY bit is located in the same place as the sign bit of many computers to simplify the polling process.

One way to poll this bit using 8080 code is as follows:

```
WAIT:   IN      STATUS      ;Input WD1002-05
                            Status register
        ANA     A           ;Update 8080 sign
                            flag
        JM      WAIT        ;Wait if BUSY (sign)
                            bit set
```

This is another way to poll the BUSY bit using PDP-11 code:

```
WAIT:   MOVB   @#STATUS,R0   ;Input status,
                             update sign flag
        BMI    WAIT          ;Wait if BUSY (N) bit
                             set
```

7.3.2 USE OF INTERRUPTS

Another, more efficient way of notifying the CPU that the WD1002-05 has completed a command is through interrupts. The INTRQ line on the WD1002-05 makes a low to high transition whenever the disk controller requires CPU intervention. This allows the Host CPU to run other tasks while the WD1002-05 is reading or writing data to the disk.

7.3.3 USE OF THE ERROR BIT

As the WD1002-05 simulates normal completions when errors have been encountered, the only way to determine Error Status is to check the Error Bit in the Status Register. The WD1002-05 error bit is so located that it can be easily tested by rotating it into the carry bit of many processors. The contents of the error register are not valid unless the Error Bit is set.

One way to check the Error bit using 8080 code is as follows:

```
        IN     STATUS        ;Get status (if not
                             already in A)
        RAR                  ;Rotate error bit into
                             C
        JC     ERROR         ;Jump if error found
```

In certain hardware configurations, the following can check the error bit using PDP-11 code:

```
        BIT    @#STATUS,#1   ;Bit test the error bit
        BNE    ERROR         ;Branch if error
                             found
```

7.3.4 USE OF THE CORRECTED BIT

Correctable errors are usually quite benign and can almost always be ignored. Some systems designers, however may wish to log their occurrence. The corrected bit has been placed in the Status Register to facilitate error logging. Correctable and fatal errors can be detected with the following 8080 code:

```
        IN     STATUS        ;Get WD1002-05
                             status
        ANI    5             ;Mask off Error and
                             Correct bits
        JNZ    SOMERR        ;Jump if we have
                             either a
                             ;correctable or fatal
                             error
```

7.4 TYPE II COMMAND PROGRAMMING

The only Type II command is the Read Sector Command. This command is characterized by the transfer of a block of data from the WD1002-05 buffer to the Host. The command features implied seek with an implicit stepping rate.

To execute a Type II single-sector command in programmed I/O mode, the system software must perform the following functions in the order shown:

1 Set up Task File and issue command with DMA bit reset (WD1002-05 will attempt to read sector)

2. Wait for Interrupt or for BUSY bit in Status Register to be reset

3. Perform a block move from WD1002-05 buffer to system memory

4. Check Error Bit in Status Register for proper completion

Note: Steps 3 and 4 above can be reversed.

To execute a Type II single or multiple sector command in DMA mode with Interrupts, the system software does the following:

1 Set up task file and issue command with DMA bit set

2. Set up DMA controller (WD1002-05 will attempt to read single or multiple sectors) (DMA controller will move data from WD1002-05 to memory)

3. Wait for interrupt from WD1002-05

4. Check Error Bit in Status Register for proper completion

Note:
The above sequence is preferred, but steps 1 and 2 above can be reversed.

7.4.1 DMA MODE

The DMA mode bit (I) in the foregoing read sector examples is a special bit in the command byte used to optimize the WD1002-05 interrupts during programmed I/O and DMA operations. If the DMA bit is reset (I = 0), the interrupt will come before the buffer is transferred. This allows a programmed I/O host to intervene and transfer the buffer of data. If the DMA bit is set (I = 1), then the interrupt will occur only after the data has been transferred. This allows the Host to go uninterrupted until the entire buffer has been transferred.

7.4.2 BLOCK MOVES

The WD1002-05 performs all transfers between itself and the disk drive through an on-board full Sector Buffer. Once the disk has been read, the data is available to the Host at any rate from DC to as high as a byte every 500 nsec. In programmed I/O applications there

is no need to consult the DRQ bit in the Status Register to determine if another byte is ready to be processed. Once an interrupt occurs or the BUSY bit is reset on a read, the Host computer should do a block move of all the bytes in the sector.

The following 8080 code demonstrates a transfer from the WD1002-05 to system memory. The transfer address is in HL and the byte count is in B:

```
READIT: IN      DATA      ;Get data from
                          WD1002-05 sector
                          buffer
        MOV     M,A       ;Store it in memory
        INX     H         ;Increment memory
                          pointer
        DCR     B         ;Decrement byte
                          counter
        JNZ     READIT    ;Do it again if whole
                          sector not xferred
```

The following Z-80 instruction does it all. The transfer address is in HL, byte count is in B and WD1002-05 data register address in C:

```
READIT: INIR              ;Transfer buffer from
                          WD1002-05 to
                          memory
```

7.4.3 USING DMA

A special bit in the Read Sector Command optimizes the WD1002-05 interrupts for DMA operation.

7.4.4 MULTIPLE SECTOR TRANSFERS

The WD1002-05 can transfer more than one sector per command, if interfaced, using DMA and interrupts. Transfers as large as an entire track can be executed. The Sector Count Register holds the number of records to be transferred (if sector count is zero, then 256 records will be transferred.) The Sector Number Register holds the starting sector of the transfer. When a multiple sector transfer is successfully completed, the Sector Count Register is equal to zero and the Sector Number Register is equal to the last sector transferred plus one.

If a fatal error is encountered during a multiple sector transfer, the Sector Number Register is left pointing to the sector that contained the fatal error, and the Sector Count Register holds the number of sectors that were not transferred.

If a correctable error is encountered during a multiple sector read, the corrected bit in the Status Register is set, but the operation is not terminated because correctable errors are not considered fatal.

7.4.4.1 Partial Sector Transfers

The WD1002-05 permits partial sector transfers on read operations. This allows the user to read the first part of a sector and discard the rest. During programmed I/O, the byte counter in the block move routine is set to the number of bytes to be read. During DMA operations, the DMA controller is set with the number of bytes to be transferred.

Normally, during a DMA read operation, the WD1002-05 interrupts the Host after a sector has been transferred. However, if only a partial sector is being read, the WD1002-05 does not know that the operation has been completed. Therefore, the 'transfer complete' interrupt must come from the DMA controller.

During write sector operations, the DMA controller will interrupt the system after the buffer has been transferred to the WD1002-05, but before the data have been written. Some systems with advanced interrupt handling capabilities can easily mask off this spurious DMA interrupt. For those systems that cannot, the WD1002-05 has a provision built into its command structure to detect read operations.

7.4.4.2 Interrupt Source Selection

Bit 4 of all commands determines whether the operation is a Read Sector operation or something else. Those commands that require the interrupt from the WD1002-05 have this bit set to 1 The Read Sector Command (the only one that might need the DMA controller's interrupt) has this bit set to a 0. Bit 3 of the command is then used to select programmed I/O interrupts or DMA type interrupts.

7.4.4.3 Clearing Hardware DRQ

During partial sector reads, the DMA controller stops the DMA transfer before the WD1002-05 has a chance to issue its last data request. Because of this, the DRQ line might be set the next time transfer parameters are sent to the DMA controller. To avoid spurious (and often fatal) DRQs, the user must do a hardware clear of the DRQ line unless another command is issued. DRQ is actually cleared by doing dummy reads of the Sector Buffer to dump the rest of the data.

7.4.4.4 Interrupt Selection Circuit

If the user is reading partial sectors with the WD1002-05 and wants to have the system automatically configure its interrupts, a circuit similar to that shown by Figure 7-1 must be implemented.

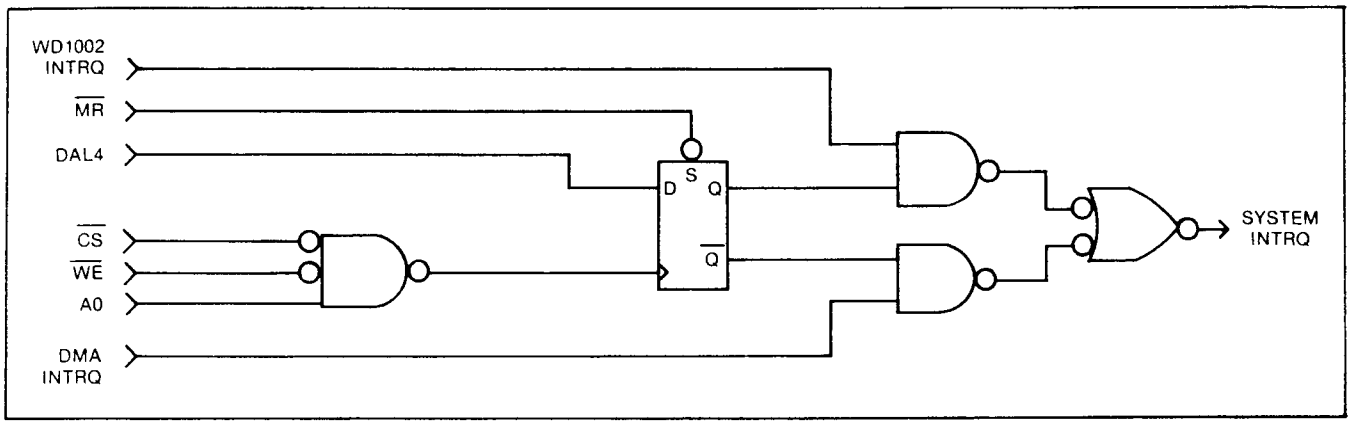


FIGURE 7-1. INTERRUPT SELECTION CIRCUIT

7.4.5 SIMULATED COMPLETIONS

All WD1002-05 commands (except multiple sector transfers) act in precisely the same manner, whether or not an error was encountered. The only way to determine whether an error has occurred is to sample the Error Bit in the Status Register. Simulated completions offer the system designer the following tangible benefits:

- Simplifies masking and generation of interrupts
- Simplifies non-error handling portions of the system software
- Eliminates the software overhead of handling different types of errors
- Simplifies system software error handling validation (any error is handled the same way as any other error)
- Prevents system failure in the event of some obscure error condition that the system programmer did not anticipate

7.5 TYPE III COMMAND PROGRAMMING

Write Sector and Format are Type III commands. These commands are characterized by the transfer of a block of data from the Host to the WD1002-05 buffer. Like the Type II commands, these commands feature implied seek with an implicit stepping rate. To execute a single sector Type III command in programmed I/O mode, the system software must go through the following functions in the order indicated:

1 Set up Task File and issue command

2. Perform block move from system memory to WD1002-05 buffer (WD1002-05 attempts to write a sector or format)
3. Wait for interrupt or for BUSY bit in Status Register to be reset
4. Check Error Bit in Status Register for proper completion

To execute a single or multiple sector Type III command in DMA mode with interrupts, the system software goes through the following steps:

1. Set up Task File and issue command
2. Set up DMA controller (DMA controller moves data from memory to WD1002-05) (WD1002-05 attempts to write sector or format)
3. Wait for interrupt from WD1002-05
4. Check Error Bit in Status Register for proper completion

Note: Steps 1 and 2 above can be reversed.

7.5.1 FORMATTING

The Format Command is very similar to the Write Sector Command, except that the Sector Buffer is filled with interleave and bad block information instead of with user data. Two bytes will be written to the buffer for each sector to be formatted.

The first (lower) byte will be either a 00 or an 80 in hex. If the lower byte is a 00, the sector is marked as good. If the lower byte is an 80, and there is any attempt to read it or write to it, the sector sets the Bad Block Bit in the Error Register. See cautions regarding media imperfections mapping in subsection 7.6 Bad Block Mapping.

The second (upper) byte is the logical sector number of the next sector to be formatted. This number is recorded on the disk.

On a 32-sector-per-track disk, 32 pairs of bytes containing formatting information must be supplied to the drive during each format operation. To start the format operation, the buffer must be completely filled, even if the sector table is not as long as the buffer. This means that on a 32-sector-per-track disk, with 64 bytes of formatting information supplied, if the sector size is 256 bytes, then 192 bytes of garbage must be passed to the controller to start the format operation.

As the contents of the Sector Buffer do not imply how many sectors are to be formatted, a dedicated register is provided. This Sector Count Register must be loaded with the number of sectors to be formatted before every format operation. To calculate the maximum number of sectors per track, see Appendix C.

7.5.2 INTERLEAVING

If sequential sectors on the disk are to be read, the next sector passes by the read/write head before a read or write can be set up. The disk then makes a complete rotation to pick up this next sector. If an attempt is made to read all 32 sectors on a particular track, it requires 32 rotations or about a half a second per 8K bytes. This performance can be significantly improved by interleaving, a technique that allows the system to read or write more than one sector per rotation.

Suppose the system takes less than three sector times (3 times 32 rotational periods with 256 byte sectors) to digest the data that it has read and to set up the next read operation. This means that if the second logical sector can be physically placed four sectors away from the first one, the controller can read it without much delay. This four-to-one interleave factor allows a potential reading of the entire track in only four rotations. In the example given, the throughput is increased by a factor of eight.

The simplest way to determine the optimum interleave for any particular system is through experimentation. If the system maintains its directories or virtual memory-swapping areas in a certain place on the disk, it sometimes makes sense to have more than one interleave.

To simplify driver software, the WD1002-05 automatically maps logical sectors to physical sectors to achieve interleave. This logical-to-physical map is recorded during the format operation on each track of the disk in the ID fields of the sectors. Table 7-2 is an example of an interleave table for a 32-sector track with 4:1 interleave and no bad blocks.

The first byte in each byte-pair in Table 7-2 is set to 00. This marks each block as a "good" block. The second byte of each byte-pair is the logical sector number. The first byte pair in Table 7-2 represents the first logical sector of the track. The underlined byte pair represents the second logical sector.

7.6 BAD BLOCK MAPPING

Winchester and thin-film-technology drives often do not have perfect media. Manufacturers allow imperfections in the media to reduce cost which consequently lowers the cost of drives.

The user of the WD1002-05 which interfaces with Winchester and thin-film-technology drives is required to map out any media imperfections. This can be accomplished in various ways, some highly operating-system dependent. Here are a few ideas:

7.6.1 SECTOR PRE-ALLOCATION

If the operating system supports random sector or group allocation, the bad blocks can sometimes be mapped out by recording an un-deletable file, using all the bad sectors on the disk. When the operating system tries to write to the bad block, it determines that the sector or group that contains the error has already been allocated. The operating system automatically maps over the bad sector.

There are some minor restrictions associated with this form of bad-block mapping: the file that contains the bad sector must never be moved to another section of the disk, the bad sector file may not be read (for obvious reasons), and reads or writes to the disk that do not consult the disk allocation map (physical reads/writes) are not allowed.

TABLE 7-2.
INTERLEAVE TABLE WITH
32 SECTORS AND 4:1 INTERLEAVE

00	00	00	08	00	10	00	18
00	01	00	09	00	11	00	19
00	02	00	0A	00	12	00	1A
00	03	00	0B	00	13	00	1B
00	04	00	0C	00	14	00	1C
00	05	00	0D	00	15	00	1D
00	06	00	0E	00	16	00	1E
00	07	00	0F	00	17	00	1F

Note: The balance of the buffer must be filled with something to start the format operation.

7.6.2 ALTERNATE TRACKS

The alternate-track method works on most operating systems but requires more software overhead. Whenever a read or write is attempted, the track number (cylinder and head select) is checked against a table maintained by the operating system or driver. If the track number matches the table, the driver knows that there is a flaw somewhere on that track and looks up the alternate track for the flawed one. The read or write is then performed elsewhere.

The primary disadvantage of this type of bad-block mapping is the high software overhead. When the system is brought up, the alternate-track table has to be read from a flawless area of the disk. After it has been read, every read or write operation must check the alternate-track table before performing its respective operation.

7.6.3 SPARE SECTORS

The spare-sector method is probably the simplest to implement in most systems. Its primary disadvantage is that at least one sector must be set aside as a spare for each track. During format, the physical sector that contains the flaw is written with some illegal sector number. The physical sector following it contains the real logical sector and its data. Table 7-3 is an interleave table that shows how the user mapped out the fifth physical sector by telling the WD1002-05 to write a logical sector number of FF to it.

Please note that when formatting the disk in this manner, at least one sector must have an illegal sector number. Also, as one sector has been allocated to bad block mapping, a sector 1F no longer exists.

TABLE 7-3.
INTERLEAVE TABLE WITH 32 SECTORS AND 4:1 INTERLEAVE — PHYSICAL SECTOR FIVE MAPPED OUT

00	00	00	08	00	10	00	18
00	FF	00	01	00	09	00	11
00	19	00	02	00	0A	00	12
00	1A	00	03	00	0B	00	13
00	1B	00	04	00	0C	00	14
00	1C	00	05	00	0D	00	15
00	1D	00	06	00	0E	00	16
00	1E	00	07	00	0F	00	17

7.6.4 BAD BLOCK BIT

The WD1002-05 allows the user to set a marker that is recorded into the ID field. When the WD1002-05 attempts to read or write a sector with a Bad-Block Mark set, the operation will be aborted and the Error Bit in the Status Register and the Bad-Block Bit in the Error Register is set. The size, head, cylinder, sector and ID CRC fields of the selected sector must be correct in order to detect a Bad-Block Mark. This means the ID field must be error-free in order to detect the Bad Block Mark.

Table 7-4 shows an interleave table where the user has marked all the sectors with a Bad-Block Mark and recorded all sectors redundantly. The interleave is not very important here, because it is assumed that the driver will not attempt to read bad sectors sequentially.

TABLE 7-4.
INTERLEAVE TABLE WITH REDUNDANT SECTORS, NO INTERLEAVE, AND ALL SECTORS MARKED AS BAD BLOCKS

80	00	80	01	80	02	80	03
80	04	80	05	80	06	80	07
80	08	80	09	80	0A	80	0B
80	0C	80	0D	80	0E	80	0F
80	10	80	11	80	12	80	13
80	14	80	15	80	16	80	17
80	18	80	19	80	1A	80	1B
80	1C	80	1D	80	1E	80	1F
80	00	80	01	80	02	80	03
80	04	80	05	80	06	80	07
80	08	80	09	80	0A	80	0B
80	0C	80	0D	80	0E	80	0F
80	10	80	11	80	12	80	13
80	14	80	15	80	16	80	17
80	18	80	19	80	1A	80	1B
80	1C	80	1D	80	1E	80	1F

SECTION 8
THEORY OF OPERATION

8.1 GENERAL

The WD1002-05 Winchester Disk Controller (WFC) is a stand-alone general purpose controller board designed to provide a buffer interface between a Host controller and up to three Winchester disk drives. The WD1002-05 is fabricated using a proprietary chip set designed specifically for Winchester Floppy disk control.

The design of the WD1002-05 circuitry implements all of the logic required for host interface, WD1002-05 internal diagnostics, variable length Sector Buffer, Task Files, ECC diagnostics and correction, data separation, and WD1002-05 control. The Winchester drive signals from the Host controller are based upon the floppy look-alike interface with the Seagate Technology ST506 and other compatible drives. All necessary drive signal decoding for the floppy disc drives is performed solely by the WD1002-05 so that the Host controller sees only Winchester drive signal format.

8.2 WD1002-05 ARCHITECTURE AND FUNCTIONAL DESCRIPTION

The internal structure of the WD1002-05, illustrated in Figure 8-1, consists of six major functional blocks as well as all necessary support logic. They are as follows:

1 Host Interface Logic (HIL)

2. Buffer Manager Control Processor (CP)

3. Error Detection and Support Logic (EDS)

4. Sector Buffer (SB)

5. Winchester Disk Drive and Buffer Interface (WDBI)

6. Floppy Disk Drive and Buffer Interface (FDBI)

The Host can communicate with the Winchester or floppy disk via the SB. $\overline{MR}$ is asserted upon power-up, which in turn causes the WD1002-05 to execute a special TEST Command that initiates internal diagnostic routines within the WD1002-05 to ensure the functionality of the WD1002-05. The internal diagnostic routines can also be exercised by the Host explicitly, in addition to five other macrocommands used to execute disk operations. The six macrocommands are as follows:

1 TEST

2. RESTORE

3. SEEK

4. READ

5. WRITE

6. FORMAT

Prior to issuing any command to the WD1002-05, the Host must first set up command parameters in the Task File registers, i.e. sector size, drive select information, sector number accessed, etc. The Host must then fill the Sector Buffer with the required data if either a Write or Format Command is to be executed by the WD1002-05. The WD1002-05 BUSY status bit is set when the Sector Buffer has been filled by the Host, or immediately upon receipt of any other type of command from the Host. The WD1002-05 then executes the command issued, at which time all communications between the Host and the WD1002-05 are suspended. The only access available to the Host is the ability to poll the status of the BUSY bit. The command issued by the Host is read by the CP from the Command Register in the Task File, interpreted, and re-issued to either the Winchester or Floppy disk processor, or executed directly by the CP. Upon completion of the command, the WD1002-05 sets the INTRQ/DRQ lines, dependant upon the type of command issued, and clears the BUSY bit. At this time, the Host can read status and error information from the Task Files before issuing another command.

8.2.1 HOST INTERFACE LOGIC (HIL)

The HIL contains the requisite logic to buffer all data/command access between the Host, the WD1002-05, the WD1010, and the WD2797 controllers. Bus protocol is exactly the same as the WD1010 Hard Disk Controller device. All data and command information is transferred on an 8-bit DAL bus. This tri-state asynchronous bus is controlled by the Host, only if the WD1002-05 is not BUSY. The Host accesses the WD1002-05 by presenting a stable address (A0-A2) along with a $\overline{RE}$ or $\overline{WE}$ strobe qualified by $\overline{CS}$. The direction of transfer is determined by the $\overline{RE}$ and $\overline{WE}$ signals. For DMA transfers, the WD1002-05 provides a DRQ signal to inform the DMA controller of a pending transfer. HIL also produced INTRQ for interrupts after commands, or to signal a transfer completion for Interrupt Driven Systems. The Host can reset the WD1002-05 by asserting $\overline{MR}$ (if $\overline{MR}$ is asserted, the WD1002-05 internal diagnostics routine is initiated and the Host must wait for BUSY to be cleared before issuing a command to the WD1002-05).

The HIL passes DATA and COMMANDS to the EDS and CP along with processed strobes derived from $\overline{WE}$, $\overline{RE}$, $\overline{CS}$, and A2-A0 signals. HIL receives DATA and STATUS from the EDS and CP along with control information concerning DRQ and INTRQ generation.

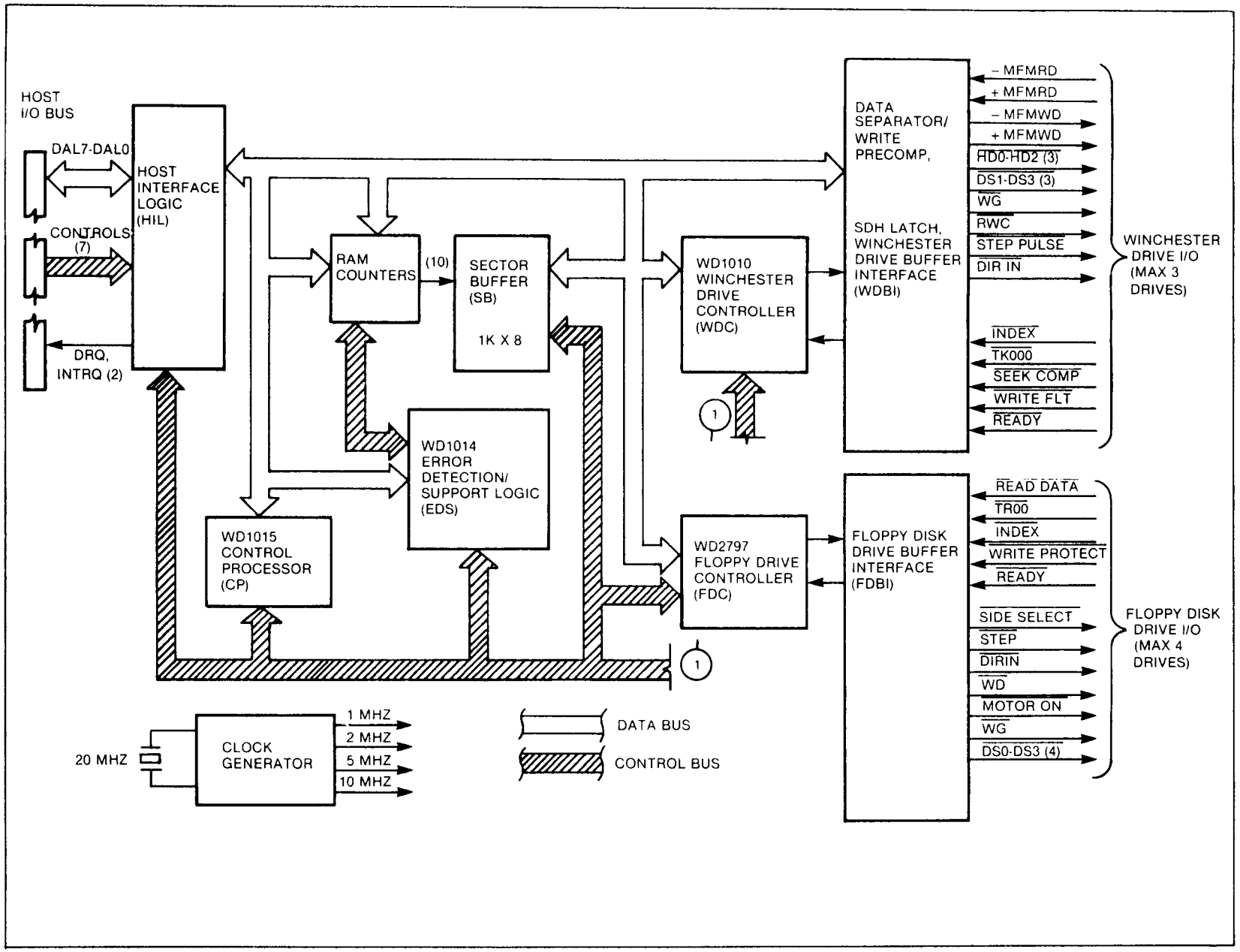


FIGURE 8-1. WD1002-05 FUNCTIONAL BLOCK DIAGRAM

8.2.2 CONTROL PROCESSOR (CP)

The main control center of the WD1002-05 is the CP (WD1015), used in conjunction with the EDS (WD1014) device, the clock generator, and the Task Files (TSF). The EDS device is the right hand of the CP and of sufficient complexity to be treated as a separate functional entity.

The CP controls the transfer of information within the WD1002-05 and maintains the necessary copies of the TSF found on both drives. Host access to the WD1002-05 causes the CP to access Task File information in the TSF after a command is issued. The TSF are physically located in the controller chips and on-board external logic is used to reflect any changes such as error and status information required to integrate the floppy format to that of the Winchester controller. Depending upon the command, the CP makes the buffer accessible to the Host, the WD1010, or the WD2797 controllers.

The CP also controls the operation of the Error Correcting logic. During the transfer of data from the Host to the WD1010, the EDS monitors the data bus, (if so enabled), to compute a 4-byte ECC which is appended to the data transferred to the WD1010 and recorded on the disk. During data transfers from the WD1010 to the Host, the CP uses the ECC to validate the data. If the data is corrupted, the CP envokes recovery techniques such as retries and correction. A maximum of eight retries are attempted if two consecutive syndromes do not match. Correction is attempted only if two consecutive syndromes match. If the error is uncorrectable, the operation is terminated.

When the CRC mode has been selected, the WD1010-05 controls the writing and checking of the CRC bytes. When an error has been detected, the WD1010-05 instructs the WD1002-05 to read the same sector again for a maximum of ten times. (For details ref. to WD1010-05 Data Sheet.)

The CP is also used to handle data transfers to and from the SF for the floppy disk controller, which only uses CRC check byte for its data fields.

During status reads by the Host, the CP consolidates the normal completion status from the WD1010, the WD2797, and the current EDS status into a form consistant with established WD1010 error reporting format. This consolidated status is then presented to the Host.

8.2.2.1 Clock Generator

The 20 MHz oscillator drives the Clock Generator which provides all timing clocks for the WD1002-05.

The crystal frequency divided by 2 is used as a reference clock (2XDR) and then divided again by 2 for a 1X clock (WCLK) which is used to clock the WD1010.

The Floppy Disk Controller (WD2797) operates with a 1 MHz clock for 5.25″ drives. 2XDR divided by 10 is used to produce the required 1 MHz clock.

The CP uses a 10 MHz clock (2XDR), giving an instruction cycle time of 1.5μs. Most instructions execute in 3.0μs, or two cycles.

8.2.2.2 Task/Syndrome File (TSF)

The TSF provides on-chip storage of the required Task Files for the WD1010/WD2797 controllers, and the 4 bytes of syndrome used for ECC. The check/syndrome bytes are physically stored in the ECC generator/checker. The WD1014 (EDS) maintains its own Command Register which serves also as an Error Register upon command completion. All other registers comprising the TSF are physically part of the WD1010 and WD2797 controllers. The CP controls all access to the TSF. Refer to separate sections on Task Files for their use.

8.2.3 ERROR DETECTION AND SUPPORT LOGIC (EDS)

The WD1014 EDS chip provides the WD1002-05 with Error Correction Capabilities (ECC) and support logic. The EDS chip is a single chip device specifically designed to add ECC to the 5.25″ Winchester disk drives. The EDS also contains three 8-bit registers, three counters, and several latches that enhance the CP capabilities for control functions in a real time operation. This 40 pin chip replaces approximately 35 TTL packages consisting of shift registers, flip-flops, and combinatorial logic gates.

8.2.3.1 Error Detection

The EDS processes all data transfers in either direction between the SB and the WD1010, if SDH bit 7 is set. This bit should only be set for hard disk operations. The EDS generates the ECC/SYNDROME bytes by using a polynomial division process which can provide unique code words for long streams of data. The polynomial selected is a computer generated code optimized for sector sizes of 128, 256, 512, and 1024 byte data fields. During Normal/Write operation, this division process produces a 32-bit remainder which is used as the four ECC bytes. In Normal/Read operation, the ECC bytes are recomputed and compared to the recorded ECC bytes to generate the Four SYNDROME bytes. If the syndrome is zero, there were no errors detected. Otherwise, the non-zero syndrome is used by the CP to compute the displacement of the error vector within the bad sector. This information is then used to correct the data if a single burst of no more than five bits in error occurred.

During a WRITELONG operation, the EDS is inhibited from computing the 32-bit ECC word. The EDS then accepts a 32-bit appendage from the Host and passes it on, unaltered, to the WD1010 to be recorded on the disk. This permits the Host to induce errors anywhere in the data stream so that the operation of the EDS can be validated during a subsequent READSHORT operation.

During a READLONG operation, the EDS is inhibited from producing a syndrome. Instead, it copies the recorded ECC check bits and passes them unaltered to the Host, appended to the sector data being read. As with WRITELONG, this command is useful when validating EDS performance.

The EDS uses a 2-bit serial implementation of the generator polynomial during ECC generation and error detection. During correction operations, a serial reverse polynomial is used by the CP to compute the error vector and displacement. Correctable errors are corrected in the buffer without Host intervention. Uncorrectable errors are reported to the Host and the uncorrected data is transferred to the Host for further action.

8.2.3.2 Support Logic

The support logic consists of two 8-bit latches (command/error register and SDH latch). Data requests, interrupts, BUSY, multiple mode, and Read Command information is also maintained and updated in the WD1014 to enhance the capability of the CP to handle control functions in real time.

The EDS controls the buffer counter, incrementing and presetting due to commands from the Host, and contains all the necessary logic to handle Sector Buffer overflow. Data, buffer addresses, and Drive/Head select control are handled by the same multiplexed 8-bit address and data bus.

8.2.4 SECTOR BUFFER (SB)

The SB is used to buffer a sector of data being transferred to or from the Host. The sector size may be programmed for 128, 256, 512, or 1024 bytes. Thus, the minimum RAM size required is 1KX8. The address counters are controlled by the CP and EDS. All control signals for SB access are provided by the WD1010, or the CP when communicating with the floppy controller (WD2797).

8.2.5 WINCHESTER DRIVE AND BUFFER INTERFACE (WDBI)

The WDBI consists of the Winchester Disk Controller (WD1010), an 8-bit SDH latch, write precomp logic (WPC), data separator, and appropriate drivers and receivers. The WD1010 is connected to the Winchester drives and the SB by means of 20 signal lines that form the WDBI. As previously mentioned, the WD1002-05 uses a multiplexed data/address bus to share SB access and control lines with the WD1010. Proper use of this interface results in having only a presettable counter to control the buffer and a latch/decoder to control up to three Winchester drives. The counter is preset using two separate strobes, one for each byte of the address, one 8-bit counter package provides addressing capability for a 128 or 256 byte sector buffer size. By using more than one counter package, the WD1002-05 permits a multiple sector buffer size of 64K bytes. The SDH latch is used to provide drive selects 1-3 and head selects 0-7.

8.2.5.1 Write Precompensation (WPC)

The generation of Modified Frequency Modulation (MFM) write data takes place in the WD1010. This device accepts a byte of data and a WCLK to produce MFM data through internal circuitry which decides when and where to write clocks and data on the data stream under the MFM encoding rules. The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as 'dynamic bit shift.'

Dynamic bit shift comes about as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error.

Write precompensation is used to reduce the effect of dynamic bit shift. It is a way of predicting which direction a particular bit shifts and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last and the present bits to be written and producing one of three signals depending on what these bits are. The three signals are $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$ and NOMINAL. They are used in conjunction with a delay line to cause the leading edge of a data or clock bit to be written earlier, later, or on time.

The processor can enable or disable the generation of these signals by controlling the Write Pre-Comp (WPC) line from the addressable latch. When WPC is high, precomp is in effect. When WPC is low, no precomp is

generated and the nominal output of the device is held true.

8.2.5.2 Data Separator

Data is recorded on Winchester disks using an MFM technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. The fact that clock bits are not recorded with every data bit cell requires circuitry that can remain in sync with data during the absence of clock bits. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bit timing when clock bits are missing and synchronize to clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier and filter to sync onto and hold a specific phase relationship to the data and clock bits in the data stream. The phase-lock occurs at 2x average data rate frequency (f_0), which in turn is used to synthesize a clock called RCLK with a frequency = $1/2\ f_0$. This synthesized clock can then be used to separate data bits from clock bits with external logic to shift the resultant serial data into registers for byte parallelization within the WD1010.

8.2.6 FLOPPY DRIVE AND BUFFER INTERFACE (FDBI)

The FDBI consists of a Floppy Disk Controller (WD2797), a drive select latch, head load, motor-on, buffer management logic, and appropriate drivers and receivers. The write precomp and data separator are internal to the WD2797. The WD1002-5 can support up to four 5.25" floppy drives, double density and single or double sided.

The principal component of the FDBI is the WD2797 Floppy Disk Controller. This device has the primary responsibility for controlling the floppy drive.

The data path between the diskette and the Host is serial between the heads and an 8-bit shift register. From here it travels parallel between the 8 bit data register and the Host via the data lines (DAL).

The location on the disk to be accessed by a read/write function is determined by the track and sector registers. The sector number is incremented as the head moves in and decremented as the head moves out. Thus the sector number reflects the present position of the head on the disk. If a different drive is about to be selected, the track number is stored for future use, and replaced with the track number that represents the current head position on the drive to be selected. This way it still represents the current track and drive.

NOTE

The stepping of the head is controlled by the WD1015.

The Sector Buffer is written into, via the DAL lines, by the Host and is compared with the sector number recorded on the disk to determine when the desired sector is found.

Generally the control of the Floppy is divided as follows:

- WD1015 controls when the head will step and in which direction.
- WD1014 selects the drive.
- WD2797 selects the side, detects the address mark, and examines the ID field, determines that the correct sector has been found, controls write precomp and data separation, reads and writes the data, and controls the CRC functions.

SECTION 9
MAINTENANCE

9.1 GENERAL

When the board is shipped from the factory, all adjustments have been made using ST506 and SA450 drives. The user need not make any adjustments if the drives supported are compatible with the forementioned drives.

There are four adjustments associated with the WD1002-05 on-board data separation/write precomp circuitry and V_{CO} that might have to be made if a drive with a different data rate is installed. On the WD2797, the write precompensation value is adjustable and the data separator might have to be adjusted for drives of different data rates.

9.2 OSCILLATOR FREQUENCY

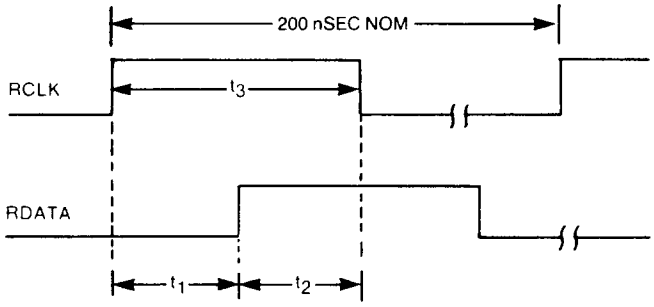
Data separation circuitry on the WD1002-05 uses a voltage-controlled oscillator (V_{CO}) which phase-locks onto incoming data and provides a clock suitable for separating data and clock bits on an MFM-encoded data stream. The V_{CO} must be adjusted using the following procedures:

Connect a frequency counter to Test Connector U30-10 (V_{CO} OUT).

Connect a DVM to Test Connector U30-1 (V_{C}i IN).

Make all connections to the board, including the Host and drive. Adjust the variable capacitor C19 until the frequency output locks onto the desired center frequency for the drive being used which is 10.000 MHz for ST506 or compatable drive. Once this "locked-on" frequency is achieved, continue the same adjustment for an input voltage of 2.5 ± 0.5 V.

To complete the adjustment, monitor RCLK and RDATA inputs to the WD1010 (U19-39,37 respectively) and fine tune variable capacitor C19 until the rising edge of RDATA is exactly centered in either Half Phase or RCLK.



$t_1 = t_2$
$t_1 + t_2 = t_3$

9.3 WD2797 ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

Strobe $\overline{MR}$ (U15-19).

Jumper across E3-E4.

Observe pulse width on WD (U15-31).

Adjust WPW (U15-33/R24) for desired pulse width (Precomp Nominal Value).

DATA SEPARATOR

Observe pulse width on TG43 (U15-29).

Adjust RPW (U15-18/R25) for 1/8 of the read clock (500 ns for 5.25" DD).

Observe frequency on DIRC (U15-16).

Adjust variable capacitor (C7) on V_{CO} pin (U15-26) for Data Rate (250 KHz for 5.25" DD)

Remove jumper between E3-E4.

NOTE

To maintain interval V_{CO} operation, insure that $\overline{TEST}$ = 1 whenever a Master Reset pulse ($\overline{MR}$) is applied.

9.4 TEST/OPERATION JUMPER VARIATIONS

1	E1 to E2	N.A.
2.	E16 to E15	N.A.
3.	E4 to E3	Normaly open. Ground for Floppy Write Precomp/Data Separator adj. only.
4.	E8/E10 to E9	GND (E8-E9) = No Write Precomp. Open = Write Precomp always. E10 to E9 = Write Precomp above TG43.
5.	E5/E7 to E6	E5 to E7 = Normal READY latch. E6 to E7 = If FRDY line available from Floppy drive.
6.	E11 to E12	GND = 40msec MOM delay. OPEN = 1 sec MOM delay.
7.	E13 to E14	N.A.
8.	E17/E19 to E18	E18 to E19 = 10 MHz. E18 to E17 = 20 MHz.
9.	E20 to E21	N.A.
10.	E22 to E23	N.A.
11	E24 to E25	N.A.